Logic Indicating Device for Troubleshooting for Non-Pulsed Output Signals of Integrated Circuits (ICs).

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ABSTRACT

Construction and testing of a Logic Indicating Device (LID) has been carried out and applied to test the circuits of Transistor-Transistor Logic (TTL) integrated circuit. Faulty nodes of integrated circuits with non-pulsed signals were readily detected, without the problem of pin shortings associated with other probe devices. An implementation algorithm for the troubleshooting process has also been developed.

(Keywords: logic indicating device, complementary metal-oxide semiconductor, CMOS, transistor-transistor logic, TTL, integrated circuits, non-pulsed signals, troubleshooting, electronics)

INTRODUCTION

In digital electronics, logic means an exact, definable relationship between the inputs and outputs of a circuit. This relationship allows a digital logic circuit to make a clearly defined decision and express that decision as an output voltage level (Schuder and Fowler, 1993). The term logic level refers to voltage levels which represent the binary digits 1 and 0 depending on the logic family of integrated circuits (ICs) used in the digital system.

In order to measure the output signal of digital circuits especially transistor–transistor logic (TTL) and complementary metal–oxide semiconductor (CMOS), the logic indicating device (LID) is used. The LID is a unique piece of test equipment designed to overcome the problem of shorting pins of ICs which is associated with the digital voltmeter and oscilloscopes. The LID can measure output logic level of TTL integrated circuits, which have voltage range between OV – 0.8V as its low level signal and voltage range between 2V – 5V, considered as high level signal. In CMOS integrated circuits, a voltage range between OV – 1.5V is considered a low level signal, and a range between 3.5V - 5V is considered a high level signal. In percentage, this is indicated in Figure 1.

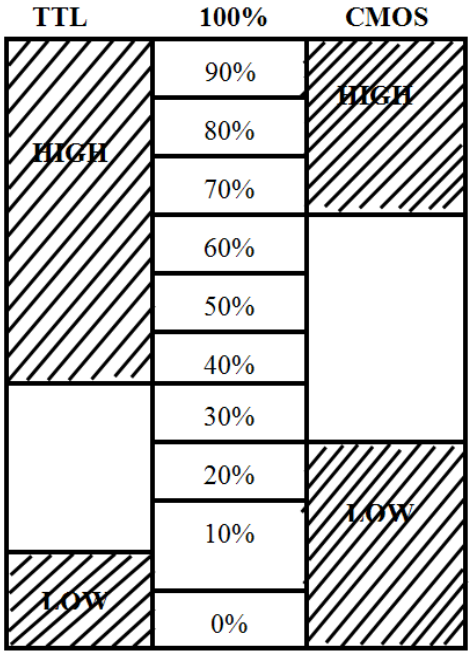


Figure 1: Logic Level in Percentage for the TTL and CMOS ICs.

The LID requires a maximum voltage of 5V which serves as the input voltage, and a frequency response of up to 1OMHZ, and a high input impedance of 300kΩ. The overview of the major steps of fabrication of CMOS processes has been previously highlighted (David et al., 2004).

The device is powered by two leads that connect to the positive and negative terminals of a power supply. When activated, the LED indicators of the LID show a green light for LOW or a red light for HIGH level signal output. The system is designed

and fabricated for troubleshooting and diagnosis of non-pulsed output signal of digital circuits, especially integrated circuits of transistor–transistor logic (TTL).

DESIGN OF THE LOGIC INDICATING DEVICE (LID)

In the design of the LID, use is made of discrete electronic components and digital integrating circuit in which the NE555N timer IC was used. The design is divided into three parts:

i. The power supply unit
ii. The power control circuit
iii. The output indicator

Assembly of the three parts produces a system whereby the output signals of digital test circuit are made possible through the control system to the output indicators where the logic levels of the signal are detected.

THE POWER SUPPLY UNIT

Power supply in every electronic device is one of the components that fail most often, and hence needs extra care in its design. This is the reason for its extra cost (Faissler, 1991). A voltage supply of 5V output is required to power the positive lead needed by the NE555N timer IC for pulse generation. The transformer used consists of two coils that are electrically insulated and arranged such that a changing magnetic field sets up an alternating electromotive force (EMF) in the secondary coils. The frequency of the 6V transformer is 50 Hertz, and the supply current and the supply voltage are a cycle out of phase. The power output is given by;

$$P = IV \cos \theta \quad \textbf{(1)}$$

where V = root mean square current,
Cos θ = the power factor.

A 240V AC enters the primary winding of the transformer and is stepped down to 6 Volts through the secondary of its winding. The output voltage which is alternating is then converted to a direct or steady voltage by four diodes in a bridge rectifier arrangement. Filtering is accomplished by using a capacitor in the circuit. The power supply circuit designed for the operation of logic indicating device is shown in Figure 2.

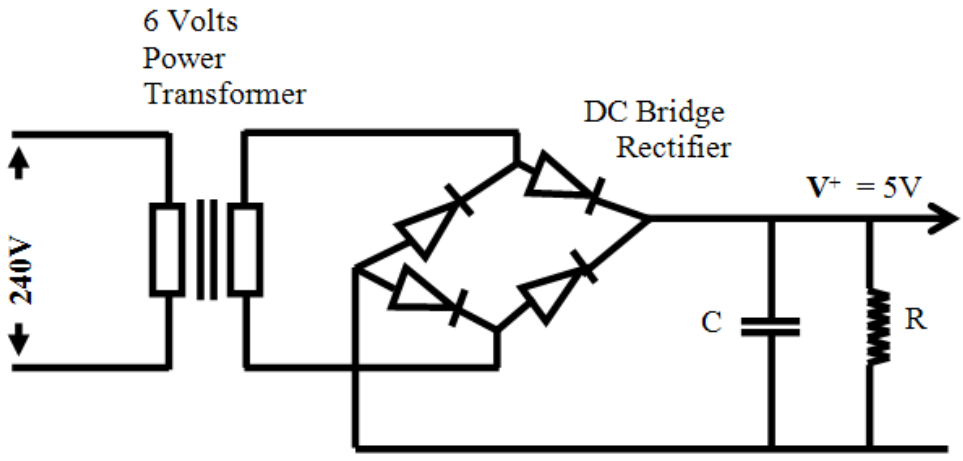


Figure 2: The Power Supply Circuit for Converting the 240 Volts AC to 5 Volts DC.

THE CONTROL UNIT

The control circuit consists of the following parts:

i. The rectifier diodes
ii. The timer circuit
iii. The limiting resistor
iv. The by pass capacitor

The Rectifier Diodes

The type of diodes used in the design of the circuit are the rectifier diodes. They have the advantage over other diode types in this circuit by having a maximum current rating from 500mA to 10Amps and also, by the fact that they offer a very a low internal voltage drop of approximately 1volt. When the control circuit is supplied with 5volts through the rectifier diode D_1 from the power supply as shown in Figure 3, the rectifier diode allows current to flow only when the voltage input is in forward direction.

The action of diodes D_2 and D_3 is that they protect the IC in the circuit from reverse polarity. The diode D_4 is connected to the chassis ground to prevent current flow in the opposite direction which may damage the circuit.

The Timer Circuit

The NE555N is used as the timer circuit in this design. 555 timer was first introduced around 1971 by Signetics Corporation as the SE555/NE555 and was the only commercial timer IC available. It uses a maze of transistors, diodes and resistors (Tony, 2006). The timer circuit is where pulse generation takes place. The output is a square waveform that is produced on pin 3 of the IC. A mark to space ratio of 1:1 and 50% duty cycle is obtained in the output of this IC. A block diagram of the NE555N IC used in the design is shown in Figure 4.

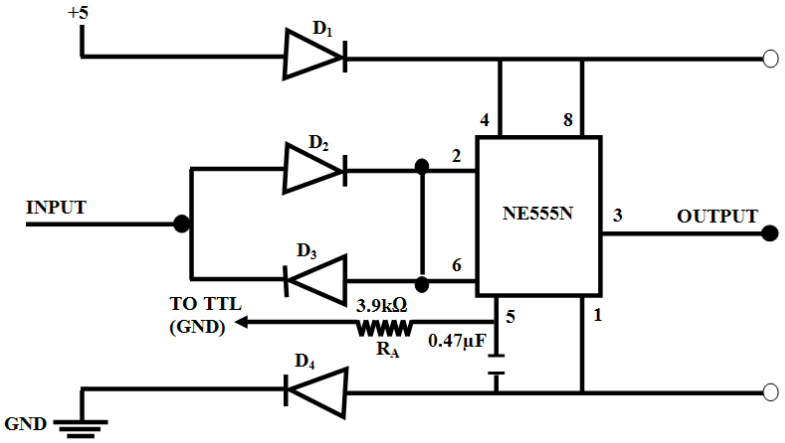
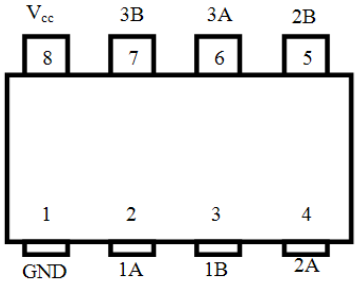


Figure 3: Diagram of Rectifier Diodes Used in the Design of the Logic Indicating Device.



1A	=	Trigger pin
1B	=	Output pin
2A	=	Reset pin
2B	=	Set pin
3A	=	Threshold voltage pin
3B	=	Discharge pin
GND	=	Ground pin
V_{cc}	=	Supply voltage pin

Figure 4: The Block Diagram of NE555N Timer IC.

The rectifier diodes D_2 and D_3 connected in reverse parallel between pins 2 and 6 in Figure 3, means that the timing capacitor can only be powered through voltage supply of the test point. Pin 5 of the NE555N IC is the set pin and is grounded through a resistor of 3.9kΩ. Pin 3 is the output pin that activates the light emitting diodes. Input power supply enters pin 8, and pin 4 allows reset of the clock after it has completed its cycle. Pin 1 is ground, and pin 7 is dormant in the design of the IC.

The time of pulse generation is given by;

$$t = C_1 R_A \, 1n \{V_{cc} / (V_{cc} - V_{th})\} \quad \textbf{(2)}$$

where V_{th} is the threshold voltage. In the internal circuitry of the NE555 N timer IC, lower and upper threshold voltages of 1/3 V_{cc} and 2/3 V_{cc} respectively, are preset on lower and upper comparators whose inputs are connected to the timing capacitor, which is charged and discharged through two resistors R_A and R_B of 3.9kΩ and 3.0kΩ, respectively.

For V_{th} = 2/3 V_{cc} equation (2) gives:

$$t = C_1 R_A \, 1n \{V_{cc} / V_{cc} (1 - 2/3)\}$$
$$= C_1 R_A \, 1n \, 3 \quad \textbf{(3)}$$

$$t = 1.0986 \, C_1 R_A \quad \textbf{(4)}$$

But C_1 charges from 1/3 V_{cc} to 2/3 V_{cc} which gives charging time interval $t_1 = t^{11}_1 - t^1_1$ as follows:

After 1/3 V_{cc},

$$t^1_1 = C_1 R_A \, 1n \{1/ (1 - 1/3)\}$$
$$= C_1 R_A \, 1n \, (3/2)$$
$$0.40053 \, C_1 R_A$$

At 2/3 V_{cc},

$$t^{11}_1 = C_1 R_A \, 1n \{1/ (1 - 2/3)\}$$
$$t^{11}_1 = C_1 R_B \text{ in } 3 = 1.0986 \, C_1 R_A$$

this implies that

$$t_1 = t^{11}_1 - t^1_1$$
$$= (1.0986 - 0.4053) \, C_1 R_A$$
$$= 0.693 \, C_1 R_A \quad \textbf{(5)}$$

Also, at 1/3 V_{cc},

$$t_2 = 0.693 \, C_1 R_B$$

This gives total time T as,

$$T = t_1 + t_2 = 0.693 \, C_1 (R_A + R_B)$$

and the frequency,

$$f = 1/T = 1.44 / \{C_1(R_A + R_B)\} \text{ Hz} \quad \textbf{(6)}$$

The Limiting Resistor

In the design of the LID, a resistor of 3.9kΩ is chosen as the value of resistance connected between pin 5 of the NE555N timer IC and the lead of TTL. Two resistors of 390Ω are connected each to the LEDs to limit the current through the LEDs to a safe levels, or high current through the LEDs may give incorrect logic levels. The two 390Ω resistor are placed in series with RED and GREEN LEDS to the output of the NE555N timer IC, that is on pin 3 as shown in Figure 5.

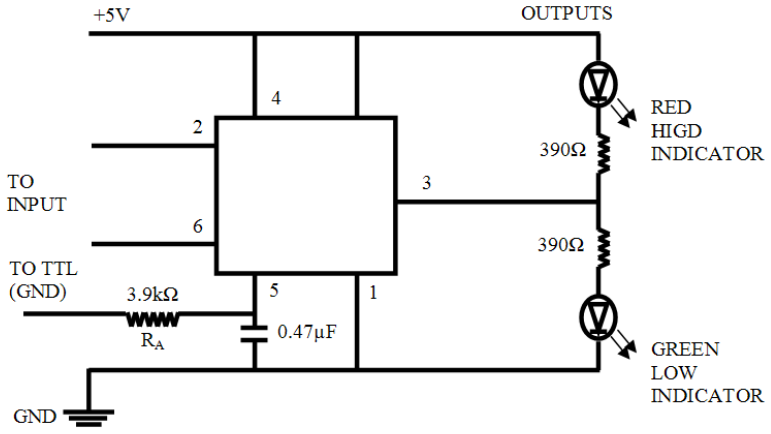


Figure 5: Diagram of NE555N Timer IC Showing Resistors Connecting to Pin Levels.

The Bypass Capacitor

The bypass capacitor smoothes the output voltage as it opposes change in voltage from high to low or low to high. The capacitor of 0.47μF charge through the low internal resistance of the conducting rectifiers. When discharging, the discharge path through the high resistance of the load in the circuit has a much longer RC time constant. Apart from smoothening voltages, the bypass capacitor used in the design of the LID prevents transient voltages from affecting the device when the TTL (GND) lead is not connected.

THE OUTPUT INDICATOR

In this work, LEDs serve as the output indicators of the LID. For the operation of LEDs, the current under forward bias is given as,

$$I = I_s\,(e^{qv/nkT} - 1) \qquad \textbf{(7)}$$

where I_s is the saturation current. The conversion efficiency is given as;

$$\eta = P_{ex}/IV \qquad \textbf{(8)}$$

where P_{ex} = output or external power, I = current, and V = voltage.

In the LID design, two 390Ω resitors are placed in series with the RED and GREEN LEDS to limit the current entering the LEDS to safe level. When low voltage appears on the test circuit, the low indicator LED will light. On the other hand, a high indicator LED will light if a high voltage is tested (Figure 5).

OPERATION OF THE LID CIRCUIT

The composite circuit shown in Figure 6. is accomplished by mounting the components on the printed circuit board. The test circuit (TTL or CMOS ICs) to be tested is first powered. The LID is then set to the TTL or CMOS lead to the ground and the other lead is left unconnected. The needle-like input is used to make contact with the test circuit and signal enters the circuit through this end and to the IC through the two diodes D_2 and D_3 connected in reverse polarity to prevent current surge entering into the IC. In the IC, current is converted to pulse signal by the IC, which acts as pulse generator and is then passed through the output pin to the LED. The output of the signal on the LED depends on the input signal and if at the input the voltages is low, a low output is indicated by a GREEN LED, while if a high voltage is received at the test point and directed through the needle like test input, a high output is obtained and is represented by a RED LED. The complete LID circuit is shown in Figure 6.

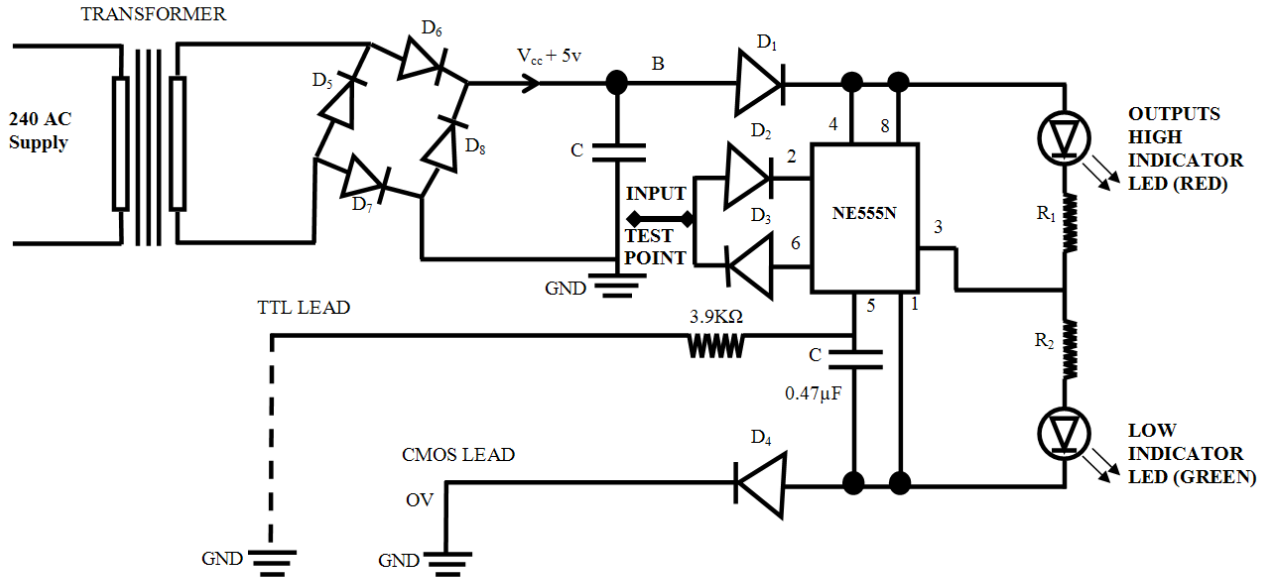


Figure 6: Complete Circuit Diagram of the Logic Indicating Device.

TESTING AND IMPLEMENTATION OF LID

The application of LID circuit in troubleshooting and diagnosis of faulty integrated circuit and the processes of implementation of the scheme are now discussed. A typical circuit containing both NAND and OR gate is shown in Figure 7.

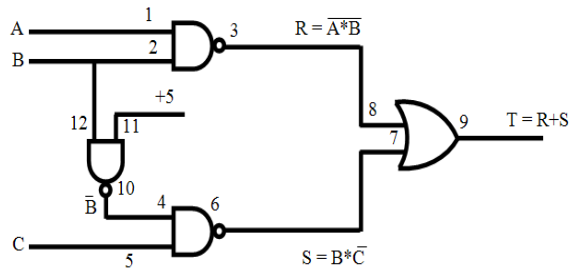


Figure 7: IC Circuit Containing NAND and OR Gate.

Table 1: Truth Table for IC Circuit Containing NAND and OR Gate of Figure 7.

A	B	C	$R = \overline{A*B}$	$S = B*\overline{C}$	T = R+S
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	1	1	1
0	1	1	1	0	1
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	0	0

The procedure involves the application of combination of HIGHS and LOWS to the circuit input by connecting a jumper wire from each input to V_{cc} or GND, and setting the jumpers from one input combination to another by the use of truth table. The logic level produced on the output by this input combination is measured. Changing the jumpers produces the next input combination in the table and the process continues. The input and output signals at the circuit input and output are direct current (dc) voltage levels.

In Figure 7, the output expression for gate R in the circuit is R = A*B, the expression for S gate is S = B*C and the expression for the entire circuit or output is T = R + S. The input on the truth table will be represented by A, B and C, while the output will be represented by T.

To test a digital circuit with LID, we first connect the three circuit inputs to GND with jumper wire to simulate the first input combination. The next step is to power the circuit and determine the output logic level. If the input combination is 000, the output will be 0 as in the truth table (Table 1). If we move to the next combination i.e. for, 001 the circuit input jumper is lifted from ground and connected to V_{cc}. The A and B inputs from the truth table are left connected to GND. If then the input combination is 001 and on further checking, the logic level on pin 4 of the output gate is correct for the input conditions, and the logic level on pin 5 of the output gate is not correct then, this automatically eliminates gate R as the cause of the problem in the circuit.

Consequently, the faulty gate S has narrowed the problem to about half of the total circuit. If the output gate had been to determine the logic levels on pins 3 and 4 inputs, finding an incorrect signal on one of the inputs would narrow the problem down to an even smaller part of the circuit. A fault on the input of the gate S again, would further narrow down the search to that part of the circuit as causing the problem.

TROUBLESHOOTING ALGORITHM FOR TTL INTEGRATED CIRCUITS

An illustration of troubleshooting with LID is performed on two TTL integrated circuits (7400 quad 2 – input NAND circuit and 7432 quad 2 – input OR circuit) shown in Figure 8.

List of parts;

7400 quad 2 – input NAND gate
7432 quad 2 – input or gate
LED: Red diffused T – 1 ¾ LED
R: ½w, 150ohms, 10% resistor.

The LED and the resistor are included to indicate the logic levels and to limit the current through the LED to a safe level respectively. The algorithmic steps taken to detect fault in the circuit are tabulated below in Table 2.

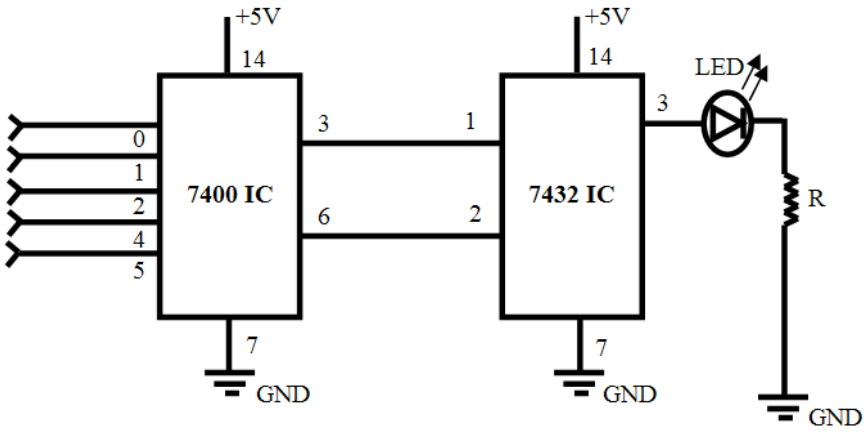


Figure 8: Diagram of 4 – Input NAND Circuit.

Table 2: Algorithm for TTL Integrated Circuit.

Step	Test	Result	Conclusion
1.	Set the indicating device to TTL and test node 1 and 2.	Both are HIGH.	7422 IC has power.
2.	Node 3 and node 6.	Both are LOW.	7400 IC has power.
3.	The state of the four – input NAND circuit.	All inputs are HIGH and indicates a HIGH output.	The state of the four – inputs NAND circuit is faulty.
4.	The outputs of the NAND gates at pins 3 and 6 of the 7400 IC.	Both outputs are LOW.	The NAND gates are in good conditions.
5.	The inputs to the OR gate at pins 1 and 2 of the 7432 IC.	Both inputs are LOW.	The OR gate input pins 1 and 2 are correct, but the output is still not correct, we conclude that the OR gate is faulty and the 7432 IC needs replacement.

CONCLUSION

A logic indicating device (LID) has been designed to provide a means of testing for non pulsed output signal of digital circuits, especially integrated circuits of transistor – transistor logic (TTL). An algorithm for implementation of the LID circuit has been illustrated in troubleshooting a faulty TTL based integrated circuits (ICs).

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