Case Study on the Profit Margin Model of Wafer-Ring Testing Handler for Semiconductors.

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ABSTRACT

Profit is the main goal of every business. Hence, investment on technology in a manufacturing firm ultimately aims at improving manufacturing efficiency to reduce manufacturing cost, thereby contributing to the profit of a firm. In this research, the author studied multi-site testing technology in the semiconductor testing industry to determine the contribution of technological advancements to profit. A profit model was developed based on economic theory with multi-site testing variables. The multi-site technology employed in this work was the wafer-ring handler, which is a popular technological approach. Five multi-site configurations were applied. These configurations were single-, quad-, octal-, ×16-, and ×32-sites. A hypothesis was analyzed by using one-way ANOVA and post-hoc test.

(Keywords: profit margin, multi-sites testing, cost of test, testing technology, theory of the firm)

INTRODUCTION

The selling price of computers has decreased by 47% over the past 20 years. Profit margin during this period was maintained by reducing fabrication cost. However, from early 2012 onwards (Bao, 2003), fabrication cost has ceased to be the deciding factor for profit margin in semiconductor manufacturing. Fabrication cost has been replaced by testing cost, as shown in Figure 1.

The cost of testing increases with the number of transistors in each chip. Thus, testing cost should be reduced in the future. The selling price of electronic devices continues to decline, thereby hindering manufacturers from maintaining profit margins and remaining competitive in the market. Thus, testing cost has become a major concern requiring urgent attention.

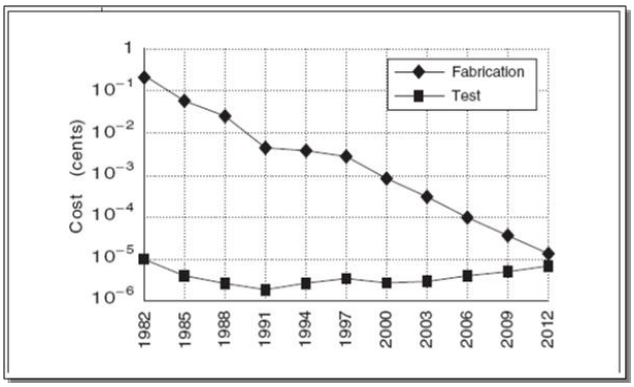

Figure 1: Cost of Testing a Transistor Approximates the Cost of Fabricating. (Bao G., 2003)

Consequently, a reduction in testing cost has become the common goal of semiconductor manufacturers worldwide. Failure to reduce testing cost can cause a semiconductor chip manufacturing company to lose its competitiveness in the market. An effective method by which to reduce testing cost is to decrease testing time. Decreasing testing time also increases testing throughput. To achieve this objective, the performance and speed of the test equipment have to be improved. Therefore, the chip-transfer time and chip-testing sequence should be developed to test semiconductor chips rapidly.

To improve the testing process, numerous new technologies have been developed. However, the advancement of technology increases capital investment in equipment. The failure of a new technology to provide the expected throughput outcome increases testing costs. Therefore, studying the efficiency of equipment in relation to capital investment is vital in ensuring that the semiconductor industry is geared toward the right direction and incurs lower costs in testing while maintaining adequate profit margins.

Numerous models for testing cost have been previously developed to calculate the capability of technology to increase testing throughput as well as to determine the actual cost involved in testing a semiconductor chip. However, these models do not consider profit margin in the calculation. Profit margin is crucial in determining the amount to spend on testing. Thus, this factor should be included in the calculation. The inclusion of profit margin in the calculation of testing cost determines the capability of the test equipment to achieve the expected testing cost. Therefore, as an initial effort to address the aforementioned research gap, this study presents a testing cost model that considers profit margin in the calculation.

DEVELOPMENT OF PROFIT MARGIN MODEL

Cost of Test Model

The cost-of-test model in this research was developed based on average cost theory, as shown in Equation 1. Average cost theory involves two elements: total cost and production output.

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}} \quad (1)$$

A. Total Cost

According to the average total cost theory, the total cost included of fixed cost and the variable cost. For the multi-sites testing aspect, the variables which affected the total cost are shown in Table 1 as below.

i. Fixed Cost

Whereby the fixed cost included of equipment depreciation cost (Dep) which contain of the tester cost and the test handler cost. Equation 2 was developed to calculate the equipment depreciation cost which span over five years from it purchase value to zero-cost.

$$\text{Dep} = \left(\frac{\text{Tester Cost} + \text{Handler Cost}}{5}\right) \div 12. \quad (2)$$

Table 1: Multi-Sites Testing Variable for Total Cost.

Total Cost	
Fixed Cost	**Variable Cost**
Depreciation Cost i. Tester Cost ii. Test Handler Cost	**Bad Parts Cost**
Direct Labor Cost i. Operator Salary ii. Technician Salary	
Overhead Cost i. Management Cost - Manager's salary - Supervisor's salary - Engineer's salary ii. Facility cost - Electricity cost, - compress air cost etc iii. Floor space cost iv. Maintenance cost - Wear and tear parts - Consumable parts etc v. Test accessories cost - Test socket/contactor - Test Load board	

The second variable which affected the fixed cost is the direct labor cost (DL). The direct labor (DL) cost is the monthly salary of employees who directly contributes to the production output, such as operators and technicians. Direct labor cost is expressed in Equation 3:

$$\text{Direct Labor Cost per month} = \left(\text{Operator salary per month} \times 3\right) + \left(\text{Technician salary per month} \times 1.5\right) \quad (3)$$

For the operator variable, each test-equipment setup requires one operator, and thus, three operators are needed each day to cover three production shifts. For one shift, only one operator is required. To standardize the equation for ease of understanding, three shifts are used in this study.

For the technician variable, one technician can support two test-equipment setups. Therefore, only a half the cost is needed per test-equipment setup. To cover three production shifts, only 1.5 technicians are needed.

Operator and technician wages are based on a report published by JobStreet.com. (Cited: 11 April 2012). In this study, the average wage is

used as a reference for the aforementioned positions.

In addition, the Overhead (OH) cost is the cost incurred during production aside from equipment depreciation and direct labor costs. Overhead cost includes the following.

- Management Cost includes the monthly wages of the manager, supervisor, and engineer, which are considered as indirect labor costs. Wages data are based on a JobStreet.com report (cited: 11 April 2012). Equation 4 shows management cost calculation:

$$\text{Management cost} = \text{Manager's Salary} + \text{Supervisor's Salary} + \text{Engineer's Salary} \quad (4)$$

- Facility Cost is the monthly utility cost of electricity, compressed air, and so on.

- Floor-Space Cost (FPS) is the cost of the area occupied by the test-equipment setup. Equation 5 shows the calculation of floor space cost:

$$\text{FPS} = \left(\frac{\text{(Selling Price)}}{3000}\right) \text{X} \begin{matrix}\text{Test Equipment}\\ \text{floor space area}\\ \text{(Sq-Ft)}\end{matrix} \quad (5)$$

In this study, the calculation of floor-space cost is based on the Malaysian Government Valuation and Property Service Department Report 2011. The 2011 "Detached House Pricing" is adopted as a reference for calculating price per sq. ft. Test equipment setup floor space costs are then calculated as the X number of area sq. ft. needed multiplied by the per sq. ft. pricing, as shown in Equation 5.

- Maintenance Cost is the cost spent in one month to maintain the test equipment, such as wear-and-tear part cost, consumable part cost, and so on. The study estimates maintenance cost at 5% per year of the test equipment cost.

- Cost-of-Test Accessories includes the test contactor and load board, which are described as follows:

  - Load Board/Probe Card is the electronic printed circuit board used for interfacing between the tester and the test handler.

  - Test Contact Socket is the mechanism used to connect the semiconductor device to the load board.

ii. Variables Cost

Another factor identified as part of the total cost calculation that has an effect on the test yield is the variable cost. From the research point of view, the variable cost is categorized as a changeable cost because it is not fixed, and it will change when the testing yield is modified.

The variable cost that needs to be included is the bad-part cost based on the test cost model developed by Rivoire (2003). The bad-part cost is imperative in this research, particularly when dealing with multi-site configurations, because the developed model will be validated using this configuration. When changes are implemented during testing, they may affect the consistency of the testing yield, which depends on multi-site repeatability efficiency.

To include the bad-part cost into the total cost equation, an equation has to be derived to calculate the cost of bad parts. The first step in deriving the bad-part cost equation is to imply the appropriate equation that can calculate the quantity of bad parts. Equation 6 is derived for this purpose.

$$\text{Number of bad part} = \text{Total Input X } \left[100\% - (\text{Testing Yield})\right] \quad (6)$$

Based on Equation 6, total incoming chip quantity is multiplied by the bad part yield, which can be obtained by deducting the testing yield from 100%. The testing yield is the tested good part percentage that can be obtained from Equation 7:

$$\text{Testing yield \%} = \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right) \quad (7)$$

Finally, to calculate the cost of the tested bad parts, the ASP of a particular type of

semiconductor chip is multiplied with the number of bad parts obtained from Equation 6. Therefore, Equation 8 is derived to determine the total cost of tested parts.

$$C_{Pkg} = ASP\left[\text{Total Input X}\left(\text{ Bad part \% }\right)\right] \quad (8)$$

where:

- C_{PKg} is the cost of bad parts;
- ASP is the average selling price;
- Total Input is the total input of semiconductor chips; and
- Bad Part % is the tested bad chips obtained by deducting the testing yield from 100%.

All costs have been discussed thoroughly to facilitate total cost calculation. Therefore, by putting together all the equations, Equation 9 is derived to demonstrate how the total cost has been integrated:

$$\text{Total Cost} = \text{Dep} + \text{DL} + \text{OH} + C_{Pkg.} \quad (9)$$

Another element incorporated in average cost theory for the developed model is production output. A detailed discussion of this element is provided in the following subsection:-

B. Production Output

Production output consists of three fundamentals: testing output (throughput), testing yield, and the equipment utilization percentage. Detailed explanations for these fundamentals are as follows.

$$UPH_{good} = \frac{3600 \text{ X N}}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1))} \text{ X}\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right) \quad (10)$$

Equation 10 was developed to calculate the production throughput whereby the throughput obtained is the tested good product by take into account the testing yield whereby the testing yield mean that the percentage of tested good. The equation of testing yield % is shown in equation 7 in this paper.

Equation 10 was integrated with the Multi-sites efficiency (MSE) as well so that the comparison between the multi-sites versus the multi-sites efficiency (MSE) can be obtained, but in this paper will not analyze of this hypothesis and will reserve for next paper publication.

To integrate the MSE into the equation, the throughput equation from Evans (1999) as shown in equation 11 need to further enhance. Following discuss step by step on how the MSE was integrated into the throughput equation.

$$UPH_{insertions} = \frac{3600 \text{ x n}}{t_{ms} + i_{ms}} \quad (11)$$

where:

- t_{ms} is the multi-site test time, that is, the time spent to complete the testing of a semiconductor chip.
- i_{ms} is the multi-site indexing time, that is, the semiconductor chip exchange time within the tested chip replaced with a new untested chip.
- n is the number of test sites, that is, the number of semiconductor chips tested in a single contact.

To achieve the integration with the MSE, the throughput equation developed by Evans (1999), shown as Equation 11, is enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as Equation 12:

$$MSE = \left(1\text{-}\frac{\Delta t}{\Delta N(t_1)}\right).100\% \quad (12)$$

where:

- Δt is the change in testing time between single-site and multi-site testing; and
- ΔN is the number of different test sites between single-site and multi-site testing.

Equation 12 is further derived, as shown in Equation 13.

$$MSE = \left(1\text{-}\frac{(t_{MS} - t_1)}{(N\text{-}1)(t_1)}\right).100\% \quad (13)$$

where:

- t_{MS} is the multi-site test time, and t1 is the single-site test time; and
- N is the number of test sites for multi-site testing.

The test handler affects testing throughput. Therefore, the test handler indexing time has to be included as part of the MSE equation. In doing so, Equation 14 is derived by including the indexing time (i), as follows:

$$MSE = 1 - \left(\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N-1)(t_1+i_1)} \right) .100\% \qquad (14)$$

For the integration of the equations to work, one must have prior understanding of the relationship between the throughputs and MSE. To determine the relationship between MSE and multi-site, the variables of MSE, which is related to the throughput, need to be understood. Equation 11 and Equation 14 show that the multi-site test time (t_{ms}) and multi-site indexing time (i_{ms}) are common variables in both equations.

In Equation 14, t_{MS} and i_{MS} represent multi-site test time and indexing time. Therefore, to clearly derive the relationship between t_{ms} and i_{ms} in relation to MSE, the integration process shown in Figure 2 is carried out.

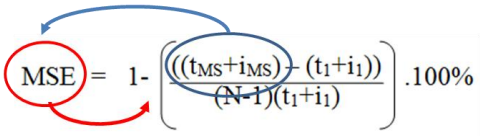

Figure 2: Deriving the Relationship between t_{ms} and i_{ms} with MSE.

As Figure 2 illustrates, t_{ms} and i_{ms} move to the left side of the equation, whereas MSE moves to the right side. The final computation for the equation of t_{ms} and i_{ms} in relation to MSE is derived and shown in Equation 15.

$$(t_{MS} + i_{MS}) = (1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1). \qquad (15)$$

Finally, Equation 15 is integrated into Equation 11 to obtain the computation for testing throughput, which includes MSE as part of the calculation. Figure 3 below shows the computation of the integration, and the complete integration is illustrated in Equation 16:

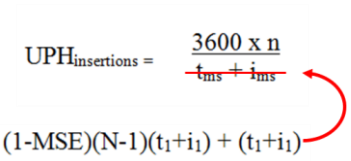

Figure 3: The Computation of the Integration of Equation 15 into Equation 11.

$$UPH_{insertions} = \frac{3600 \text{ X } N}{((1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1)),} \qquad (16)$$

where:
$UPH_{insertions}$ are represented by the testing output in one hour.

C. Equipment Utilization (U)

Equipment utilization percentage refers to the percentage by which the test equipment is used in producing output. When the test equipment is 100% utilized, then no cost is lost. The aforementioned cost refers to the total cost, as indicated in Equation 9. When equipment utilization achieves a higher percentage, the cost becomes cheaper. By contrast, when utilization percentage begins to decrease, then the cost increases (Horgan, 2004).

Given that equipment utilization percentage affects the total cost, then the former must be included in Equation 9. Therefore, the total cost equation, which involves equipment utilization percentage, is depicted in Equation 17.

$$\text{Total Cost per month} = \frac{\left(\text{Dep} + \text{DL} + \text{OH} + C_{Pkg} \right)}{\text{U}} \qquad (17)$$

The total cost obtained from Equation 17 is the monthly testing expenditure. However, the testing throughput is calculated based on the hourly production output. Therefore, to obtain the total cost per hour, Equation 17 has to be further derived, as shown in Equation 18.

$$\text{Total Cost per hour} = \frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + C_{Pkg}}{729.6} \right)}{\text{U}} \qquad (18)$$

Where the total cost is divided by 729.6 to obtain the hourly cost; and 729.6 is the total number of production hours in one month.

After all the equations and variables for average cost theory are defined, the next step is to integrate all the equations into average cost theory to derive the cost of the model. The integration is illustrated in Figure 4:

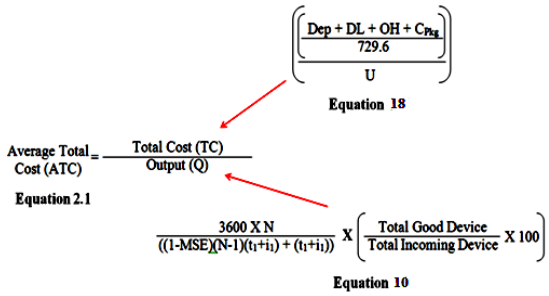

Figure 4: The Integration of Equations 18 and 10 into Equation 1.

As shown in Figure 4, the average cost in Equation 1 is integrated with Equation 18, which is the total cost in one hour, and Equation 10, which is the total number of good chips tested in one hour.

The final cost of test model is then integrated, as shown in Equation 19:

$$CPU_{GOOD} = \frac{\left(\frac{\left(\frac{Dep + DL + OH + CPkg}{729.6}\right)}{U}\right)}{\left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))}\right) \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)} \quad (19)$$

Cost of Test Profit Model

Following further discuss of the cost of test into the Profit Theory whereby the Economic Profit Theory is shown in equation 20:

$$\text{Profit} = \text{Total Revenue (TR)} - \text{Total Cost(TC)} \quad (20)$$

As shown in Equation 20, two elements are incorporated in profit calculation, namely, total cost and total revenue. Total cost can be derived from the cost of test model (Equation 19). Total revenue is discussed in this section. To clearly explain the profit margin model, the discussion is divided into three subsections. The first subsection explains how total cost is derived from Equation 19. A discussion of the total revenue follows in the second subsection. The final section discusses the development process of the cost-of -test profit margin model.

i. Total cost from Equation 19

As indicated in Equation 1, the total cost is one of the elements of the average cost. The average cost equation is used to derive the relationship of the total cost with the cost of test because the cost of test equation is based on average cost theory. The derivation process is shown in Figure 5.

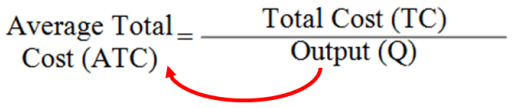

Figure 5: Deriving the Total Cost through Equation of Average Cost.

As shown in Figure 5, to derive the total cost equation through average cost theory, the output has to move from the left side of the equation to its right side, and the dividend becomes the multiplier. The total cost formula in the relation to the average is derived and shown in Equation 21.

$$\text{Total Cost} = \text{Average Total Cost} \times \text{Output.} \quad (21)$$

As discussed earlier, the cost of test is equal to the average cost; therefore, Equation 21 is further derived and expressed as Equation 22.

$$\text{Total Cost} = \text{Cost of Test} \times \text{Output.} \quad (22)$$

The total cost is equal to the cost of test multiplied by the production output, which, in this case, is the testing throughput. The variables in Equation 19 and Equation 10 are integrated with Equation 22, as illustrated in Figure 6, and further derived as shown in Equation 23.

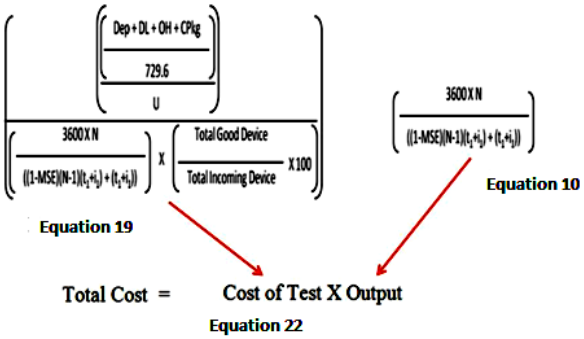

Figure 6: The Integration of Equation 19 and Equation 10 into Equation 22

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right) \Big/ \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)+(t_1+i_1))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)\right) \times \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)+(t_1+i_1))}\right) \quad (23)$$

Equation 23 is further simplified by canceling the unit per hour (UPHinsertion) equation, as shown in Equation 24.

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right) \Big/ \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)+(t_1+i_1))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)\right) \times \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)+(t_1+i_1))}\right) \quad (24)$$

The final equation for the total cost calculation is shown as Equation 25.

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right) \Big/ \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right) \quad (25)$$

Equation 25 indicates that the equipment utilization percentage and the good unit yield influence the total cost. After deriving the total cost equation, the discussion of total revenue theory in the following section:

ii. Total Revenue

Based on theory of the firm, total revenue is derived from market demand quantity multiplied by product selling price (McKenzie, 2006). This relationship is expressed in Equation 26.

$$\text{Total Revenue} = \text{Demand} \times \text{Selling Price}. \quad (26)$$

Demand refers to the quantity of semiconductor chips needed by the market, and the selling price is the ASP for a particular semiconductor chip. For this study, demand is determined as the same value of the testing throughput for easy calculation.

Both elements that influence profit have been discussed, and the following section describes in detail the development process of the cost of test profit margin model.

iii. Development Process of the Cost-of-Test Profit Margin Model

Profit is the difference between the total cost and the total revenue (Kling, 2005). The profit equation can be expressed as Equation 20 where the profit is equal to the total revenue minus the total cost.

Based on Equation 20, Equation 25 and Equation 26 are integrated, as shown in Figure 7; and the final test profit margin model is developed, as shown in Equation 27.

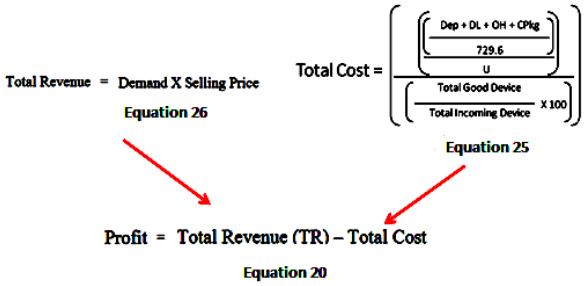

Figure 7: The Integration of Equation 26 and Equation 25 into Equation 20.

$$\text{Profit} = \left(\text{Demand X Selling Price}\right) - \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right) \Big/ \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right) \quad (27)$$

The integration is successfully shown in Equation 27, thus enabling calculation of the profit margin of the cost of testing for research hypothesis.

Changing the demand and testing throughput to produce the required demand affects the test equipment utilization percentage and the required test equipment to produce that demand, therefore Equation 27 needs to be further improved to solve this problem. The following discussion of the equations considers the utilization percentage and the change in the number of test equipment when the required demand is modified.

To simulate different production outputs or required demands, calculating the equipment utilization percentage based on testing output increment across different test-site setups is necessary.

The total cost is affected by the equipment utilization percentage and good unit yield. Therefore, the equipment utilization percentage for the different testing throughputs can be calculated using Equation 28.

$$\text{U\% for Production Output (U\%O)} = \frac{\text{Production Output}}{\text{UPH}_{\text{insertion}}\ \text{(Perfect Condition)}} \times 100, \quad (28)$$

where:
The production output (required market demand) is divided by $UPH_{insetion}$ in perfect condition. $UPH_{insertion}$ in perfect condition indicates that the maximum testing throughput that the test equipment can produce in one hour can be obtained with Equation 16 via 100% MSE.

However, Equation 16 cannot provide an accurate calculation because when the test equipment is 100% utilized, it requires an additional setup to produce the additional testing throughput. To solve this problem, the utilization percentage equation in Equation 28 should be further enhanced, as shown in Equation 29.

$$\text{Actual U\% for Production Output (AU\%O)} = \frac{\text{U\%O}}{\text{Number of Test Equipment}} \quad (29)$$

where the actual utilization percentage (AU%O) can be calculated by dividing the utilization percentage per output (U%O) with the number of test-equipment setups needed to produce the required testing output so that the actual utilization percentage per test-equipment setup can be obtained.

When the first test equipment reaches 100% utilization, additional test equipment is needed to produce the additional testing output, and the increment of the number of test equipment depends on the required output.

To obtain the cost of good unit based on the increment of testing output demand, the actual utilization percentage (AU%O) and the required number of test equipment (NOTE) have to be integrated into the total cost in Equation 25. The integration shown in Figure 8 and the new total cost equation, which considers the AU%O and NOTE, are derived in Equation 30.

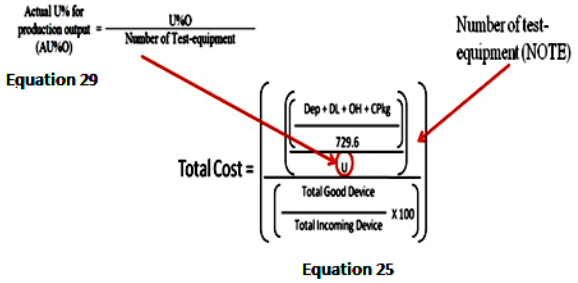

Figure 8: The Integration of Actual Utilization Percentage and NOTE into Equation 25.

$$\text{Total Cost} = \frac{\left(\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6}\right) \text{X NOTE}\right)}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100}\right)}, \quad (30)$$

where NOTE is the number of test-equipment setups needed for a particular production output, and the utilization percentage (U) is replaced with the actual utilization percentage based on the required output (AU%O).

Finally, the profit margin equation, which includes AU%O and NOTE, is derived, as shown in Equation 31:

$$\text{Profit} = \left(\text{Demand X Selling Price}\right) - \frac{\left(\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6}\right) \text{X NOTE}\right)}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100}\right)} \quad (31)$$

WAFER-RING TEST HANDLER

The concept of the wafer-ring testing handling is similar to that of the lead frame strip testing. However, this handling method attaches the lead frame on top of the wafer ring. A photograph of the wafer-ring is shown in Figure 9. This testing method is used on lead-less packagers such as wafer-level packaging, ball-guided assembly, chip scale packaging, and so on.

Similar to lead frame strip-testing handling, the semiconductor chip is tested without singulating the chip from the leadframe. As shown in Figure 10 below, the process flow is basically similar to that of leadframe strip- testing handling, the only difference being the wafer ring, which is attached to the two leadframes, is transferred to the Test Area by pick-arm 1 and attached to the test chuck.

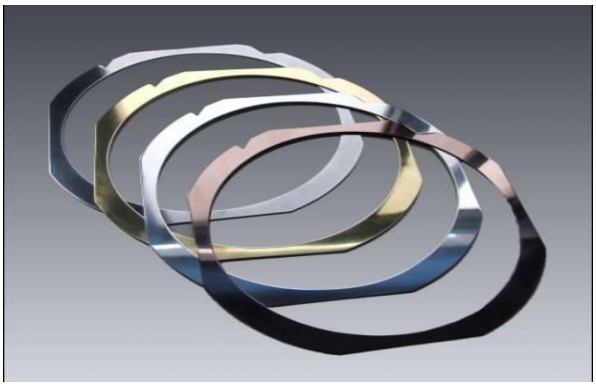

Figure 9: Example of Wafer Rings

The test chuck then transfers the wafer ring to the Test Area and, similar to the lead-frame testing handling, the wafer is punched to connect to the test socket/contactor. The test chuck moves in X and Y directions to test the entire chip on the wafer ring. The completely tested wafer ring is transferred to the output area by pick-arm 2. A photograph of the wafer ring test chuck is shown in Figure 11.

The test site configuration setup for the case study is explained in the subsequent section.

The wafer-ring test equipment can support the configuration of X32-sites. Wafer-ring testing attaches two lead frames on a wafer ring. Test site configurations are on the lead-frame layout for the setting from a single-site to X32-sites.The top-view illustration of the lead frame is shown in Figure 12,

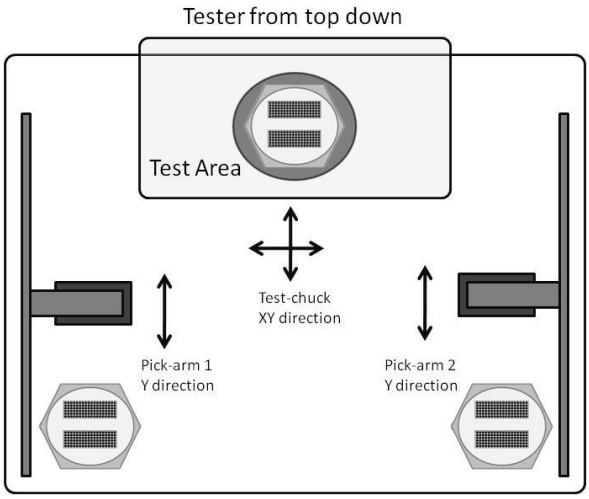

Figure 10: The Process Flow of the Wafer-Ring Testing-Handling Test Equipment.

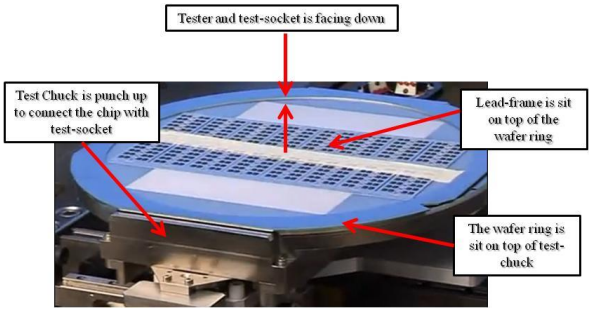

Figure 11: The Test Chuck of the Wafer-Ring Testing Handling.

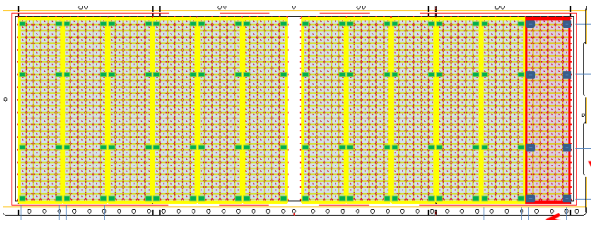

Figure 12: Top View Illustration of the Lead Frame.

For single-site testing, the wafer-ring test equipment is configured to allowcontact with one chip (represented by a bluebox) on the leadframe per touchdown, and is indexed to the next chip in the direction of the red arrow,as shown in Figure 13 below. The test equipment completes testing the entire chip in the first row before moving on to the second row to perform the same sequence.

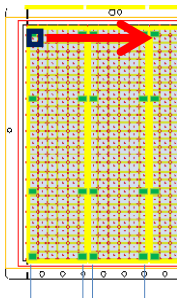

Figure 13: Single-site Testing Sequence for Wafer Ring Testing.

The sequence for quad-site testing is similar to that for single-site testing. However, the test equipment comes in contact with four chips per touchdown, as shown in Figure 14 below. After testing the first four chips, the equipment will then index toward the direction of the red arrow. After testing the first row, the equipment will continue testing the second row by following the same sequence.

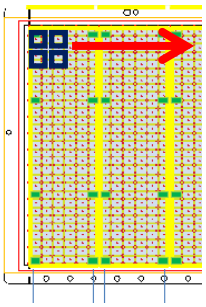

Figure 14: Quad-sites Testing Sequence for Wafer Ring Testing

Octal-site, X16-site, and X32-site testing have a sequence similar to that of single-site and quad-site testing. However, for octal-site testing, the test equipment comes in contact with eight chips per touchdown, followed by 16 chips per touchdown for X16-site testing, and 32 chips per touchdown for X32-site testing, as shown in Figures 15, 16, and 17, respectively.

After defining the test-site configuration for both types of test equipment, the next step is to decide the indexing time and test-time data collection area for the test equipment.

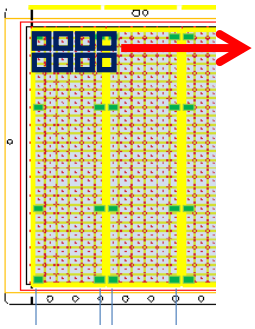

Figure 15: Octal-sites Testing sequence for Wafer-Ring Testing.

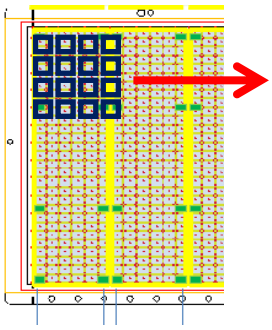

Figure 16: X16-sites Testing Sequence for Wafer-Ring Testing.

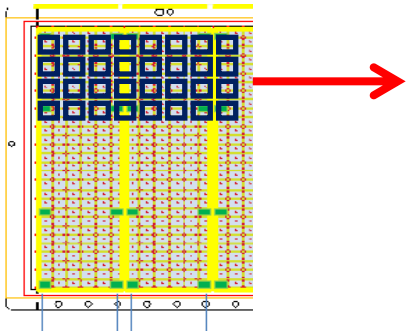

Figure 17: X32-sites Testing Sequence for Wafer-Ring Testing.

This study only considers the pure indexing time and rejects any indexing time that causes a slow down because of external factors such as wafer-ring transferring process, loading-and-unloading process, equipment jamming, and so on. Production data are only accepted if no external factors such as handler downtime, tester downtime, and others are found.

This study only focuses on the area marked by the red circle in Figure 18.

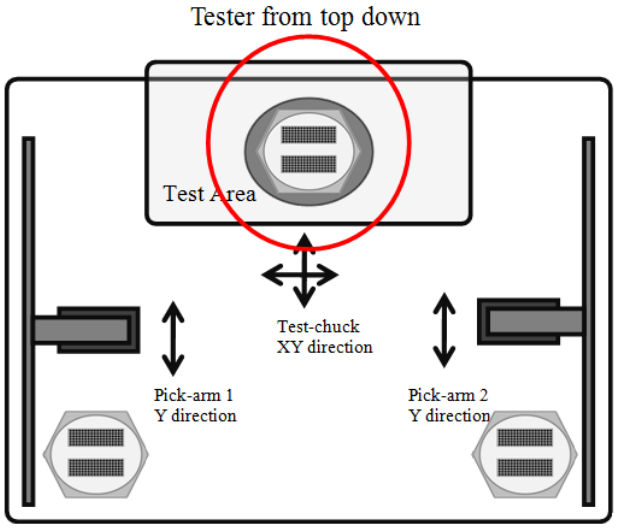

Figure 18 Focus of the Research Area.

The indexing time is considered valid when the wafer-ring is within the red circle. Once the wafer-ring gets outside the red circle for the wafer-ring exchange, the delay time for the exchange is no longer considered because it is an external factor. Otherwise, if the wafer-ring test equipment stops because of any external factors such as jamming, equipment downtime, time of handler and tester, new production lot loading, unloading time, and others, then the indexing time is not considered valid.

The test-time is considered valid if no external factors, such as tester downtime and chip contacting problems, cause a high rejection rate of the chip being tested.

To collect sufficient data for the cost-of-test, data size of the 30 sets of production lots for each test site configuration (single-site, quad-sites, octal-sites, X16-sites, and X32-sites) has to be collected (the data type to be collected is discussed in the following section). Each set of data contains 100 trial runs of the test-equipment setup, and thus, the 30 sets of data contain 3,000 test equipment trial runs. Five test-site configurations are employed in the case study; therefore, 30 sets are used for each test-site setup. The five types of test-site configurations contain 150 sets of data, including 15,000 trial runs on test equipment.

ANALYSIS RESULT

Cost of Good Unit

The fixed costs for this case study are tabulated in Table 2:

Table 2: The Fixed Costs.

Variables	Cost (RM)
Depreciation Cost/month	55417
Direct Labor Cost/month	7843
Overhead Cost/month	37613

The cost of bad parts is calculated using Equation 8, which involves an ASP of RM4.95 for the logic device. The cost of bad parts is affected by the testing yield. The summary of the cost of bad parts is shown in Table 3.

Table 3: The Cost of Bad Parts.

Test-Site Configurations	Cost of Bad Parts
Single-site	RM50.53
Quad-sites	RM68.69
Octal-sites	RM74.48
X16-sites	RM99.25
X32-sites	RM84.90

The testing Throughput results for Wafer-ring Test-Equipment are summarized in Table 4 below:-

Table 4: Testing Throughput for wafer ring Test-Equipment.

Test-Site Configurations	Throughput
Single-site	3365
Quad-sites	4626
Octal-sites	4702
X16-sites	4736
X32-sites	4390

Testing yield is one of the factors affecting the cost-of-test. Testing yield percentage data collected from the wafer-ring test-equipment setup is shown in Table 5.

Table 5: Average Testing Yield %.

Test-Site Configurations	Average Testing Yield
Single-site	99.70%
Quad-sites	99.70%
Octal-sites	99.68%
X16-sites	99.58%
X32-sites	99.61%

After obtained all the required variables, the cost of good units is calculated using Equation 19 whereby the summary is tabulated in Table 6.

Table 6: Cost of Good Unit.

Test-site Configurations	Cost of Good Unit (RM)
Single-site	RM0.0412
Quad-sites	RM0.0304
Octal-sites	RM0.0303
X16-sites	RM0.0311
X32-sites	RM0.0355

Following section discuss the data analysis through the one way ANOVA and Post Hoc Test.

An alpha level of 0.05 is used for the analysis. As previously discussed, five independent levels of configurations (a) are selected, namely, single-site, quad-sites, octal-sites, X16-sites, and X32-sites. Each independent level contains 30 data sets (n). In this case, the following data are determined:-

a = 5 independent levels,
n = 30 sets of data,
N = 150.

Therefore, the degrees of freedom are calculated as

dfBetween= 5 -1 = 4,
dfWithin = 150 – 5 = 145,
dfTotal= 150 – 1 = 149.

From the degrees of freedom between and within, which is (4,145), refer to the F-Table, with the critical value obtained as 2.3719. As indicated in the previous chapter, if the F-value is smaller than the critical value, then the null hypothesis is accepted; otherwise, the null hypothesis is rejected.

Refer to Table 5 for the summary of the cost of good unit for Wafer-ring test equipment for all test-site configurations. An analysis of the hypothesis is provided in the following sections:-

The hypothesis for the cost of good-unit analysis is as follows.

H0: Improvement of the test site has no effect on cost of good unit.

H1: Improvement of the test site has an effect on cost of good unit.

The dependence level for cost of good unit is rated on a scale of 1 to 10 and it is shown in Table 7 below:-

Table 7: Scale of Cost of Good-Unit Dependence Level.

Cost of Good Unit	Scale
0.0435	10
0.0420	
0.0419	9
0.0404	
0.0403	8
0.0388	
0.0387	7
0.0373	
0.0372	6
0.0357	
0.0356	5
0.0341	
0.0340	4
0.0326	
0.0325	3
0.0310	
0.0309	2
0.0294	
0.0293	1
0.0279	

The dependence level for the cost of good unit is scaled at level one, as the cheapest cost of good unit from RM0.0279 per chip, to level ten, as the highest cost of good unit at RM0.0435 per chip. Level increment resolution is RM0.0016, as shown in Table 7.

Table 8: ANOVA Results for Cost of Good Unit.

ANOVA Table

	SS	df	MS	F
Between	1058.173	4	264.543	872.452
Within	43.96667	145	0.30322	
Total	1102.14	149	7.397	

The one-way ANOVA results for the wafer-ring test equipment are shown in Table 8 with the F-value at 872.45, which is higher than the critical value of 2.3719. Thus, the analysis suggests a rejection of the null hypothesis and acceptance of the alternative hypothesis, that is, improvement of test sites has an effect on the cost of good unit for the wafer-ring test equipment. Thus, a post hoc test is conducted to analyze the difference among test sites.

Table 9: Post Hoc Test Analysis Results for Cost of Good Unit.

Post Hoc Test

Independence Level	F-value	Analysis Result
Single vs. Quad	583.133	Different - Reject the null hypothesis
Single vs. Octal	617.597	Different - Reject the null hypothesis
Single vs. X16	490.859	Different - Reject the null hypothesis
Single vs. x32	201.189	Different - Reject the null hypothesis
Quad vs. Octal	0.495	No Difference - Accept the null hypothesis
Quad vs. X16	3.971	Different - Reject the null hypothesis
Quad vs. X32	99.282	Different - Reject the null hypothesis
Octal vs. X16	7.269	Different - Reject the null hypothesis
Octal vs. X32	113.793	Different - Reject the null hypothesis
X16 vs. X32	63.541	Different - Reject the null hypothesis

The post hoc test analysis results for the wafer-ring test equipment are shown in Table 5.47. Only the quad-sites and the octal-sites do not have significant cost of good-unit improvements. Analysis of the results shows that the octal-sites exhibit higher improvements compared with the single-site testing. Thus, the octal-site configuration produces the chip at the cheapest cost among the test-site configurations, followed by the quad-site configuration. The X16-sites produce the second highest cost of goods unit, and the X32-sites configuration incurs the most expensive testing cost among all test-site configurations.

Cost of Test Profit

After obtaining the cost of testing for the entire test-site setup, the next step is to calculate the profit margin for the Wafer-ring test equipment.

The main elements involved in the profit-margin calculation are total revenue and total cost, as shown in Equation 20. Total revenue is calculated by the selling price multiplied by the selling output. In this study, the ASP list published by the World Semiconductor Trade Statistics and identified by Turley (2009) is used in the total-revenue calculation. The device-type used in this Case Study is the logic semiconductor, and the selling price is USD 1.50, which is equivalent to RM4.95 per chip.

Refer to table 6, the cost of good unit for wafer-ring single-site testing is RM0.0412 per chip, whereas that for quad-site configuration is cheaper by approximately 26.38%, and only requires RM0.0304 to test a single chip. The cost of good unit for octal-site configuration is slightly cheaper by 0.05%, compared with that for quad-site testing. The cost of good unit for the X16-site configuration is lower by approximately 2.46% compared with quad-site and octal-site configurations. However, the cost of good unit for the X32-site configuration is 14.28% higher compared with that for X16-site configuration. Profit margin is computed after the cost-of-testing for each test-site configuration is obtained.

The study needs to simulate mass production cost to obtain the profit margin for the test-equipment setup. To achieve this, the total cost of the production output from 1,000 to 23,000 chips per hour is calculated based on Equation 31.

In the first step in simulating the mass production cost of test, this study determines the number of test equipment needed to test the required production output across all test-site configurations. The number of test equipment is determined by referring to the utilization percentage of the test equipment. Once the utilization percentage reaches more than 100%, then additional test equipment is needed. The

utilization percentage based on the production output is calculated using Equation 28.

The number of test equipment needed and the actual utilization percentage are calculated for the wafer-ring test equipment using Equation 29 and shown in Table 10 and Figure 19.

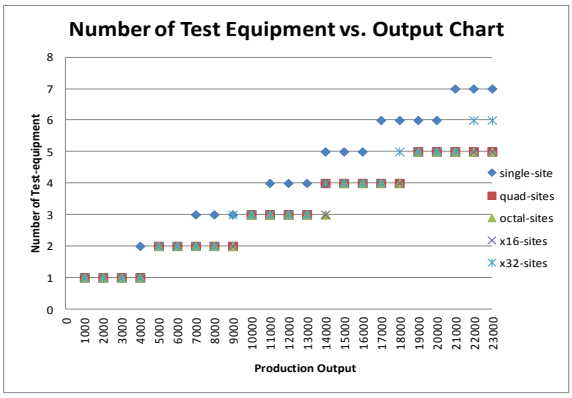

Figure 19: Number of Test Equipment Based on Production Output Increment Chart.

Figure 19 shows that the single-site and the X32-site configurations have the highest number of handler-increment configurations. The graph above also shows that the quad-site, octal-site and X16-site configurations are equally steady and that the X16-site configuration exhibits less increase among the test sites because it has the highest number of testing throughput.

The cost-of-test for the entire production output simulations across test-site configurations for the wafer-ring handler are shown in Table 11 below:-

The cost-of-test for the production output simulations, shown in Table 11, shows that the single-site configuration requiring RM0.0542 to test a single chip, making it the most expensive test-site configuration among all the configurations. This is followed by the X32-site configuration, which requires RM0.0526 per chip. The X16-site configuration requires RM0.0471 per chip, whereas the octal-sites require RM0.0454 per chip. The data show that the quad-site configuration is the cheapest test-site configuration, costing only RM0.0451 per chip.

The profit margin summary is shown in Table 12, which shows that the quad-site configuration is the most profitable setup with 99.09% profit margin, followed by the octal-site configuration at 99.08%. The third most profitable configurations are the X16-site and the single-site configurations with the same profit margin of 98.91%. Similar to the pick- and-place test equipment, the X32-site configuration has the lowest profitability.

From the case study, a conclusion can be drawn that the cost-of-test can be reduced and the profit margin can be increased in two ways, that is, either by reducing the total cost or increasing production output. A discussion of the scenarios is provided in the following paragraphs.

Scenario 1:
The average cost is lower when the total cost is decreased and production output remains the same.

Scenario 2:
The average cost is lower when the total cost remains the same but the production output increases.

Scenario 3:
The average cost decreases significantly when the total cost decreases and production output increases.

The ideal scenario for reducing the cost of test is 3. In practice, however, this scenario is difficult to achieve because additional test accessories, such as test contactors, are needed to increase production output, and additional equipment increases total costs.

In this section, the cost-of-test model and the cost-of-test profit-margin model are successfully validated.

Hypothesis: Multi-site versus Profit Margin Improvement

Refer to Table 12 for the Wafer-ring test-equipment profit summary for the production output simulation from 1,000 to 23,000. Analysis for the hypothesis is provided in the following sections:-

The hypothesis for the profit-margin analysis is as follows:

Number of Test Equipment

Test-site / Output	single-site			quad-sites			octal-sites			x16-sites			x32-sites		
	Ultilization %	Actual Utilization % per handler	Number of Handler	Ultilization %	Actual Utilization % per handler	Number of Handler	Ultilization %	Actual Utilization % per handler	Number of Handler	Ultilization %	Actual Utilization % per handler	Number of Handler	Ultilization %	Actual Utilization % per handler	Number of Handler
1000	30%	30%	1	22%	22%	1	21%	21%	1	21%	21%	1	23%	23%	1
2000	59%	59%	1	43%	43%	1	43%	43%	1	42%	42%	1	46%	46%	1
3000	89%	89%	1	65%	65%	1	64%	64%	1	63%	63%	1	68%	68%	1
4000	119%	59%	2	86%	86%	1	85%	85%	1	84%	84%	1	91%	91%	1
5000	149%	74%	2	108%	54%	2	106%	53%	2	106%	53%	2	114%	57%	2
6000	178%	89%	2	130%	65%	2	128%	64%	2	127%	63%	2	137%	68%	2
7000	208%	69%	3	151%	76%	2	149%	74%	2	148%	74%	2	159%	80%	2
8000	238%	79%	3	173%	86%	2	170%	85%	2	169%	84%	2	182%	91%	2
9000	267%	89%	3	195%	97%	2	191%	96%	2	190%	95%	2	205%	68%	3
10000	297%	99%	3	216%	72%	3	213%	71%	3	211%	70%	3	228%	76%	3
11000	327%	82%	4	238%	79%	3	234%	78%	3	232%	77%	3	251%	84%	3
12000	357%	89%	4	259%	86%	3	255%	85%	3	253%	84%	3	273%	91%	3
13000	386%	97%	4	281%	94%	3	276%	92%	3	274%	91%	3	296%	99%	3
14000	416%	83%	5	303%	76%	4	298%	99%	3	296%	99%	3	319%	80%	4
15000	446%	89%	5	324%	81%	4	319%	80%	4	317%	79%	4	342%	85%	4
16000	475%	95%	5	346%	86%	4	340%	85%	4	338%	84%	4	364%	91%	4
17000	505%	84%	6	368%	92%	4	362%	90%	4	359%	90%	4	387%	97%	4
18000	535%	89%	6	389%	97%	4	383%	96%	4	380%	95%	4	410%	82%	5
19000	565%	94%	6	411%	82%	5	404%	81%	5	401%	80%	5	433%	87%	5
20000	594%	99%	6	432%	86%	5	425%	85%	5	422%	84%	5	456%	91%	5
21000	624%	89%	7	454%	91%	5	447%	89%	5	443%	89%	5	478%	96%	5
22000	654%	93%	7	476%	95%	5	468%	94%	5	465%	93%	5	501%	84%	6
23000	684%	98%	7	497%	99%	5	489%	98%	5	486%	97%	5	524%	87%	6

Table 10: Increment of Test Equipment Units Based on Production Output.

Total Cost

Output	single-site	Average Cost	quad-sites	Average Cost	octal-sites	Average Cost	x16-sites	Average Cost	x32-sites	Average Cost
1000	MYR 465.32	MYR 0.47	MYR 647.27	MYR 0.65	MYR 668.21	MYR 0.67	MYR 693.88	MYR 0.69	MYR 681.70	MYR 0.68
2000	MYR 232.66	MYR 0.12	MYR 323.63	MYR 0.16	MYR 334.11	MYR 0.17	MYR 346.94	MYR 0.17	MYR 340.85	MYR 0.17
3000	MYR 155.11	MYR 0.05	MYR 215.76	MYR 0.07	MYR 222.74	MYR 0.07	MYR 231.29	MYR 0.08	MYR 227.23	MYR 0.08
4000	MYR 465.32	MYR 0.12	MYR 161.82	MYR 0.04	MYR 167.05	MYR 0.04	MYR 173.47	MYR 0.04	MYR 170.43	MYR 0.04
5000	MYR 372.26	MYR 0.07	MYR 517.81	MYR 0.10	MYR 534.57	MYR 0.11	MYR 555.10	MYR 0.11	MYR 545.36	MYR 0.11
6000	MYR 310.21	MYR 0.05	MYR 431.51	MYR 0.07	MYR 445.48	MYR 0.07	MYR 462.58	MYR 0.08	MYR 454.47	MYR 0.08
7000	MYR 598.27	MYR 0.09	MYR 369.87	MYR 0.05	MYR 381.84	MYR 0.05	MYR 396.50	MYR 0.06	MYR 389.55	MYR 0.06
8000	MYR 523.48	MYR 0.07	MYR 323.63	MYR 0.04	MYR 334.11	MYR 0.04	MYR 346.94	MYR 0.04	MYR 340.85	MYR 0.04
9000	MYR 465.32	MYR 0.05	MYR 287.67	MYR 0.03	MYR 296.98	MYR 0.03	MYR 308.39	MYR 0.03	MYR 681.70	MYR 0.08
10000	MYR 418.79	MYR 0.04	MYR 582.54	MYR 0.06	MYR 601.39	MYR 0.06	MYR 624.49	MYR 0.06	MYR 613.53	MYR 0.06
11000	MYR 676.83	MYR 0.06	MYR 529.58	MYR 0.05	MYR 546.72	MYR 0.05	MYR 567.72	MYR 0.05	MYR 557.76	MYR 0.05
12000	MYR 620.43	MYR 0.05	MYR 485.45	MYR 0.04	MYR 501.16	MYR 0.04	MYR 520.41	MYR 0.04	MYR 511.28	MYR 0.04
13000	MYR 572.70	MYR 0.04	MYR 448.11	MYR 0.03	MYR 462.61	MYR 0.04	MYR 480.38	MYR 0.04	MYR 471.95	MYR 0.04
14000	MYR 830.93	MYR 0.06	MYR 739.73	MYR 0.05	MYR 429.57	MYR 0.03	MYR 446.06	MYR 0.03	MYR 779.09	MYR 0.06
15000	MYR 775.53	MYR 0.05	MYR 690.42	MYR 0.05	MYR 712.76	MYR 0.05	MYR 740.14	MYR 0.05	MYR 727.15	MYR 0.05
16000	MYR 727.06	MYR 0.05	MYR 647.27	MYR 0.04	MYR 668.21	MYR 0.04	MYR 693.88	MYR 0.04	MYR 681.70	MYR 0.04
17000	MYR 985.38	MYR 0.06	MYR 609.19	MYR 0.04	MYR 628.91	MYR 0.04	MYR 653.06	MYR 0.04	MYR 641.60	MYR 0.04
18000	MYR 930.64	MYR 0.05	MYR 575.35	MYR 0.03	MYR 593.97	MYR 0.03	MYR 616.78	MYR 0.03	MYR 946.81	MYR 0.05
19000	MYR 881.66	MYR 0.05	MYR 851.67	MYR 0.04	MYR 879.23	MYR 0.05	MYR 913.00	MYR 0.05	MYR 896.98	MYR 0.05
20000	MYR 837.57	MYR 0.04	MYR 809.08	MYR 0.04	MYR 835.27	MYR 0.04	MYR 867.35	MYR 0.04	MYR 852.13	MYR 0.04
21000	MYR 1,085.74	MYR 0.05	MYR 770.55	MYR 0.04	MYR 795.49	MYR 0.04	MYR 826.04	MYR 0.04	MYR 811.55	MYR 0.04
22000	MYR 1,036.39	MYR 0.05	MYR 735.53	MYR 0.03	MYR 759.33	MYR 0.03	MYR 788.50	MYR 0.04	MYR 1,115.52	MYR 0.05
23000	MYR 991.33	MYR 0.04	MYR 703.55	MYR 0.03	MYR 726.32	MYR 0.03	MYR 754.21	MYR 0.03	MYR 1,067.02	MYR 0.05

Total Output	Average Cost per Chip				
276000	single-site	quad-sites	octal-sites	x16-sites	x32-sites
	MYR 0.0542	MYR 0.0451	MYR 0.0454	MYR 0.0471	MYR 0.0526

Table 11: Summary of Total Cost of the Production Output Simulation.

Profit

Output	single-site	Profit per chip	quad-sites	Profit per chip	octal-sites	Profit per chip	x16-sites	Profit per chip	x32-sites	Profit per chip
1000	MYR 4,484.68	MYR 4.48	MYR 4,302.73	MYR 4.30	MYR 4,281.79	MYR 4.28	MYR 4,256.12	MYR 4.26	MYR 4,268.30	MYR 4.27
2000	MYR 9,667.34	MYR 4.83	MYR 9,576.37	MYR 4.79	MYR 9,565.89	MYR 4.78	MYR 9,553.06	MYR 4.78	MYR 9,559.15	MYR 4.78
3000	MYR 14,694.89	MYR 4.90	MYR 14,634.24	MYR 4.88	MYR 14,627.26	MYR 4.88	MYR 14,618.71	MYR 4.87	MYR 14,622.77	MYR 4.87
4000	MYR 19,334.68	MYR 4.83	MYR 19,638.18	MYR 4.91	MYR 19,632.95	MYR 4.91	MYR 19,626.53	MYR 4.91	MYR 19,629.57	MYR 4.91
5000	MYR 24,377.74	MYR 4.88	MYR 24,232.19	MYR 4.85	MYR 24,215.43	MYR 4.84	MYR 24,194.90	MYR 4.84	MYR 24,204.64	MYR 4.84
6000	MYR 29,389.79	MYR 4.90	MYR 29,268.49	MYR 4.88	MYR 29,254.52	MYR 4.88	MYR 29,237.42	MYR 4.87	MYR 29,245.53	MYR 4.87
7000	MYR 34,051.73	MYR 4.86	MYR 34,280.13	MYR 4.90	MYR 34,268.16	MYR 4.90	MYR 34,253.50	MYR 4.89	MYR 34,260.45	MYR 4.89
8000	MYR 39,076.52	MYR 4.88	MYR 39,276.37	MYR 4.91	MYR 39,265.89	MYR 4.91	MYR 39,253.06	MYR 4.91	MYR 39,259.15	MYR 4.91
9000	MYR 44,084.68	MYR 4.90	MYR 44,262.33	MYR 4.92	MYR 44,253.02	MYR 4.92	MYR 44,241.61	MYR 4.92	MYR 43,868.30	MYR 4.87
10000	MYR 49,081.21	MYR 4.91	MYR 48,917.46	MYR 4.89	MYR 48,898.61	MYR 4.89	MYR 48,875.51	MYR 4.89	MYR 48,886.47	MYR 4.89
11000	MYR 53,773.17	MYR 4.89	MYR 53,920.42	MYR 4.90	MYR 53,903.28	MYR 4.90	MYR 53,882.28	MYR 4.90	MYR 53,892.24	MYR 4.90
12000	MYR 58,779.57	MYR 4.90	MYR 58,914.55	MYR 4.91	MYR 58,898.84	MYR 4.91	MYR 58,879.59	MYR 4.91	MYR 58,888.72	MYR 4.91
13000	MYR 63,777.30	MYR 4.91	MYR 63,901.89	MYR 4.92	MYR 63,887.39	MYR 4.91	MYR 63,869.62	MYR 4.91	MYR 63,878.05	MYR 4.91
14000	MYR 68,469.07	MYR 4.89	MYR 68,560.27	MYR 4.90	MYR 68,870.43	MYR 4.92	MYR 68,853.94	MYR 4.92	MYR 68,520.91	MYR 4.89
15000	MYR 73,474.47	MYR 4.90	MYR 73,559.58	MYR 4.90	MYR 73,537.24	MYR 4.90	MYR 73,509.86	MYR 4.90	MYR 73,522.85	MYR 4.90
16000	MYR 78,472.94	MYR 4.90	MYR 78,552.73	MYR 4.91	MYR 78,531.79	MYR 4.91	MYR 78,506.12	MYR 4.91	MYR 78,518.30	MYR 4.91
17000	MYR 83,164.62	MYR 4.89	MYR 83,540.81	MYR 4.91	MYR 83,521.09	MYR 4.91	MYR 83,496.94	MYR 4.91	MYR 83,508.40	MYR 4.91
18000	MYR 88,169.36	MYR 4.90	MYR 88,524.65	MYR 4.92	MYR 88,506.03	MYR 4.92	MYR 88,483.22	MYR 4.92	MYR 88,153.19	MYR 4.90
19000	MYR 93,168.34	MYR 4.90	MYR 93,198.33	MYR 4.91	MYR 93,170.77	MYR 4.90	MYR 93,137.00	MYR 4.90	MYR 93,153.02	MYR 4.90
20000	MYR 98,162.43	MYR 4.91	MYR 98,190.92	MYR 4.91	MYR 98,164.73	MYR 4.91	MYR 98,132.65	MYR 4.91	MYR 98,147.87	MYR 4.91
21000	MYR 102,864.26	MYR 4.90	MYR 103,179.45	MYR 4.91	MYR 103,154.51	MYR 4.91	MYR 103,123.96	MYR 4.91	MYR 103,138.45	MYR 4.91
22000	MYR 107,863.61	MYR 4.90	MYR 108,164.47	MYR 4.92	MYR 108,140.67	MYR 4.92	MYR 108,111.50	MYR 4.91	MYR 107,784.48	MYR 4.90
23000	MYR 112,858.67	MYR 4.91	MYR 113,146.45	MYR 4.92	MYR 113,123.68	MYR 4.92	MYR 113,095.79	MYR 4.92	MYR 112,782.98	MYR 4.90

Total Output	Profit per Chip				
276000	single-site	quad-sites	octal-sites	x16-sites	x32-sites
	MYR 4.90	MYR 4.90	MYR 4.90	MYR 4.90	MYR 4.90
	98.91%	99.09%	99.08%	99.05%	98.94%

Table 12: Profit Summary for the Production Output Simulation.

H0: Improvement of the test site has no effect on the improvement of the profit margin.

H1: Improvement of the test site has an effect on the improvement of the profit margin.

Table 13: ANOVA Results for Profit Margin.

ANOVA Table

	SS	df	MS	F
Between	0.40	4.00	0.10	0.04
Within	287.57	110.00	2.61	
Total	287.97	114.00	2.53	

The degree of freedom between is 4 and 110, with an alpha level of 0.05. The critical value obtained is 2.4542 (www.danielsoper.com/statcalc3/calc.asp.Cited: 8 September 2012).

As shown in Figure 13, the one-way ANOVA for the profit analysis shows that the F-value is 0.04, which is lower than the critical value of 2.4542. In this case, the null hypothesis is accepted and improvement in the test sites for the wafer-ring test-equipment setup is concluded to have no significant effect on profit- margin improvements.

CONCLUSION

The validation process provides evidence that increments in the number of test sites do not necessarily result in reduction in cost-of-test and improvement of the profit margin. The case study show that increasing the number of test sites does not guarantee an improvement to throughput, cost of testing, and profit margin. The main reasons for such this scenario are presented in Figure 20.

Testing throughput is the main contributor to the cost of testing and profit margin. Testing throughput is affected by the indexing time and test time. Figures 20 above show that although the indexing time for the Wafer-ring test-equipment setup steadily increases but the test time for the test equipment increases significantly once it reaches higher test-site configuration. Therefore, the test time is the root cause of the decrease in testing speed and the reduction in testing throughput, which result in an increase in testing cost, and consequently, a decrease in profit margin.

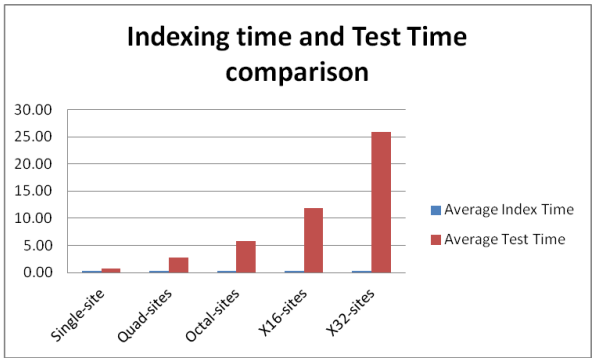

Figure 20: Comparison of the Indexing Time and Test Time for the Wafer-Ring Test Equipment.

Thus, this study concludes that simply increasing the number of test sites is not sufficient to improving testing throughput. Instead, the test time should also be reduced. The test time can be reduced in a number of ways, such as reduced pin-count testing and concurrent test among others.

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SUGGESTED CITATION

Khoo, V.C. 2014. “Case Study on the Profit Margin Model of Wafer-Ring Testing Handler for Semiconductors”. *Pacific Journal of Science and Technology*. 15(1):149-167.

Pacific Journal of Science and Technology