Improving the Portability of Water: The Water Level Equilibrator Option.

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ABSTRACT

Water is a basic necessity of life. The supply is recommended to be portable and within the reach of any and every premises. The concept of the water level equilibrator (WLE) is based on the need for effective reticulation of water in homes and also the protection of the electric pump against operation in dry or waterless sources. The WLE design so presented follows logic principles and it is a synchronous system which prohibits any control ambiguity and protects the water scheme from monitoring inadequacies and errors.

(Keywords: WLE, portability, truth table, logic, pump, PCB)

INTRODUCTION

Water is an essentially ingredient of life. All known forms of life depend on water (Water, 2009). It has basically no substitute. Government at various levels has made some efforts towards providing this all important product to its citizens. Notwithstanding, many people are still struggling to get hold of this vital product, which is an indication that efforts made by government are not good enough. Thus people, who are conscious of this basic necessity of life and have the resources to complement government efforts, go all out to create the facility and enjoy the comfort of portable water supply in their premises.

The Water Level Equilibrator (WLE) is a device that will enable a domestic water supply scheme to be automated. It guarantees the comfort of a home by ensuring that water is supplied regularly at all times. Above all, it offers protection to the scheme against running the lift pump dry-when water is not available at source. Since it enables the water scheme to be automated, human error and negligence which is common in manual control systems are eliminated in the WLE environment.

Keeping this in view, this present work attempts to develop the Algorithm System Mechanism (ASM), Flow Chart, and Truth Tables from where the logic circuit of WLE is developed.

DESIGN PARAMETERS

WLE is a device intended to automate the supply of water in any premises to ensure regular supply of portable water when desired conditions are met.

The conditions are;

(1) Pump must be activated automatically to pump water into overhead (destination) reservoir if and only if.
(a) The water in the overhead reservoir has been used up below the low level sensor.
(b) Presence of water is sensed at the source. The source here could be the water supply pipeline of the supply authority or a surface tank or underground tank/bore hole.

(2) Pump must stop when in a lift mode:
(a) The water has risen to the upper level(or tank full) sensor, or
(b) Water is exhausted at source i.e. presence of water is no longer sensed at the source of the supply.

Design Procedure

The procedure adopted in this present study is strictly based on logic principles. Where discrete components are employed, they are configured to generate the required logic

signals for system performance. Truth tables were also developed from where minimal expressions are gotten, yielding logic circuits with minimum number of gates or literals. The designed circuit is simulated using NI Multisim Version 11 to confirm workability of design and conformity with design specifications.

The Water Sensor Design

Water has relative conductivity. The conductivity of water is dependent on its level of impurities (Water, 2009). Impurities in this circumstance refer to the other substance(s) inherent in the water making its composition more than just two molecules of hydrogen and one molecule of oxygen. Pure water is hardly a good conductor but the water we use in our premises is hardly that pure and therefore presents a certain amount of conductivity. It is this conductivity characteristic of water that has been exploited in this design of water sensors. The additional advantage of the sensor under design is its improved sensitivity, which will enable it to sense water of varying range of purity.

Also use is made of the high gain and comparator characteristics of the Operational Amplifier (op-amp). Thus potential difference across the probes in water is compared with a reference voltage. The output of this comparator has the form of logic "1" if water is sensed; and logic "0" if otherwise. For simplicity of circuit power supply design and a reduction in component count, a single rail quad op-amp (LM 324) is considered in this work.

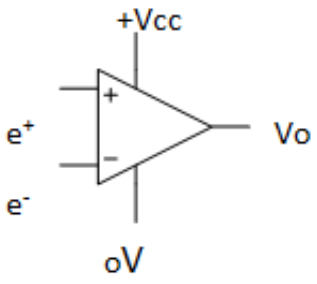


Figure 1: The Block Diagram of an Op-Amp.

Figure 1 in comparator mode, has the following characteristics; when $e^+ > e^-$, Vo ≈ Vcc, similarly when $e^+ < e^-$, Vo ≈ 0V. Where e^- is the potential at the inverting input, and e^+ is the potential at the non-inverting input which in this design is the reference voltage input (V_{ref}).

It is therefore desired that the presence of water across the sensor probes in water will cause the potential at e^- to drop below the set reference voltage (V_{ref}) causing the output voltage (Vo) to be virtually at Vcc which is considered logic "1". Similarly, the absence of water across the probes will create an open circuit effect, making the potential at e^- higher than the V_{ref} and the output voltage (Vo) at approximately zero potential (considered as logic "0").

Consider two resistors (R_1 and R_w) in series and the potential drop across R_w when the resistive circuit is connected to a voltage source V.

$$V_{RW} = \frac{R_W}{R_1 + R_W} \times V \quad \ldots \quad (1)$$

$$V_{RW} \approx V (when\ R_W \gg R_1)$$

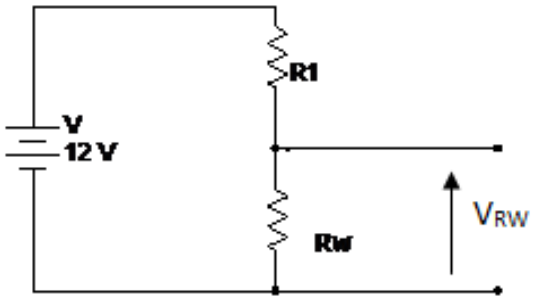


Figure 2: Shows V_{RW} - The Potential Difference across R_w in a Series Circuit.

The above situation is similar to the condition, when there is no water across the probes of the sensor – an open circuit condition that makes the resistance of R_w = infinity (∞). Similarly $V_{Rw} < V$ if $R_w < R_1$.

Thus the smaller the value of Rw relative to R_1, the smaller the value of V_{RW}. This situation is similar to the condition when the sensor senses water. The value of R_w will depend on the level of purity of water. The purer the water, the higher the potential across R_w and V_{RW} tends to rise towards V. Applying this concept in the sensor circuit; we have the model represented in Figure 3.

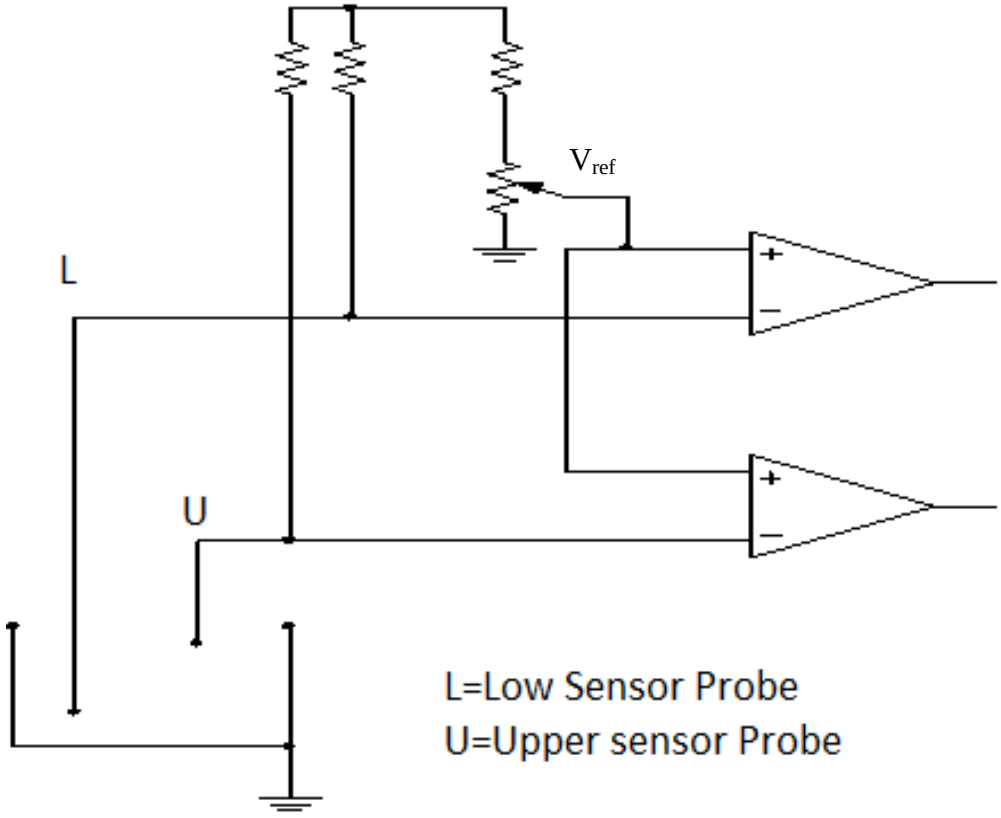


Figure 3: The Circuit Diagram of a Two-Level (Upper and Lower) Water Sensor.

Setting the Reference Voltage

The sensitivity of the water sensor is controlled by the set reference voltage.

From Equation 1, the higher the purity of water, the higher is the value of R_w and also the potential drop (V_{Rw}) across it when the sensor senses water. Since it is required that $V_{Rw} <$ Vref whenever water is sensed. The set Vref becomes a measure of the sensitivity of the sensor. Thus the nearer Vref is to V, the higher the sensitivity of the sensor. A variable resistor may be used to preset the value of applied V_{ref}.

The Logic Control Circuit Design

The logic control circuit design started with the development of the system control flow chart. The flow chart of the WLE is conceived of from the specifications given for the design and it is shown in Figure 4.

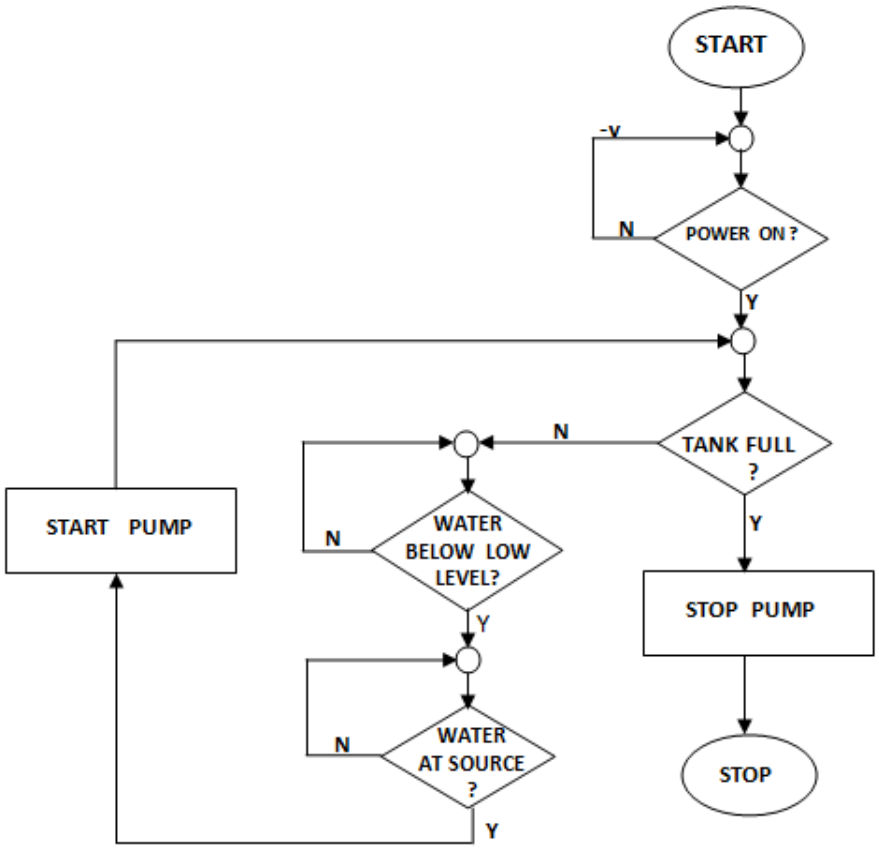


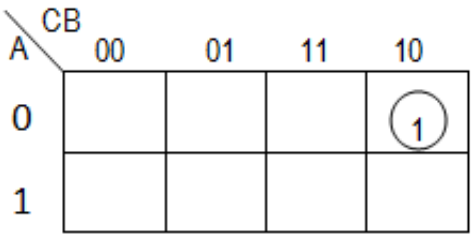
Figure 4: Flow Chart of WLE.

Based on the operational specifications of the WLE, an S-R flip flop as a latch is required to hold every control command till such command is completely executed. The S – R flip flop is considered as one of the building blocks (Floyd,2009). The next concern is to develop the logic circuit that will generate the Set(S) and Reset (R) pulses needed to routinely drive the flip flop from the truth table of the WLE controller. The truth table of the control circuit is shown on Table1.

By the application of Karnaugh map technique (Floyd, 2007), the expressions for the Set (S) and Reset (R) were obtained thus:

a) For the Set (S) input generator, and using the sum of products (SOP) formation:

Set (S) = f_{CBA} $=\sum(4)$ **(2)**



An essential subcube that gives the expression:

$$S = C\bar{B}\bar{A} \quad \textbf{(3)}$$

The set (S) input logic circuit is shown in Figure 5(a).

Table 1: Truth Table of the Control Circuit.

INPUTS			OUTPUTS		COMMENTS
C	B	A	SET(S)	RESET(S)	
0	0	0	0	0	No water in both overhead tank and at source
0	0	1	0	1	There is water at low level of overhead tank, but non at upper level and source.
0	1	0	0	1	There is water at upper level of overhead tank but not at low level and source (not practicable)
0	1	1	0	1	Overhead tank is full, but no water at source or reservoir
1	0	0	1	0	There is water at source, but overhead tank is empty
1	0	1	0	0	There is water at source, and there is water also at low level not at upper level.
1	1	0	0	0	There is water at source, and at upper level of overhead tank but no water at low level (not practicable)
1	1	1	0	1	There is water at source and overhead tank is full

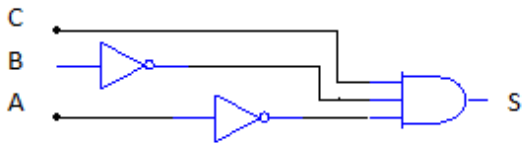


Figure 5(a): The Set(S) Input Logic Circuit.

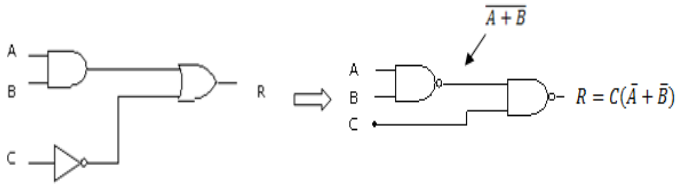
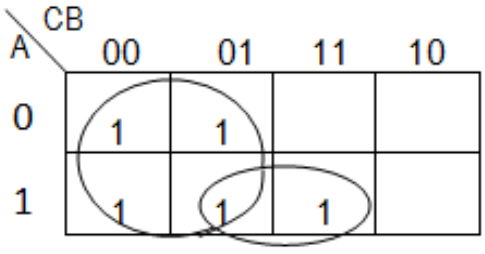


Figure 5(b): The Reset (R) Input Logic Circuit

b) For the Reset (R) input generator, and adopting SOP formation.



Reset (R) = $f_{CBA} = \sum(0,1,2,3,7)$ **(4)**

$$R = \bar{C} + BA \quad \textbf{(5)}$$

The Reset (R) input logic circuit is shown in Figure 5(b).

To make the WLE controller synchronous for improved stability and reliability, it is considered cost effective to generate the synchronising clock pulse(s) from the S and R input combinations. The truth table for the clock pulse generator is shown in Table 2.

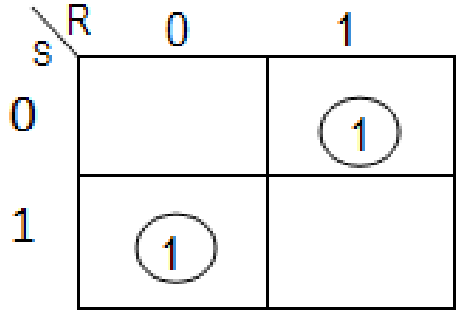
Table 2: Truth Table of Synchronizing Pulse Generator.

Inputs	Output	Remarks
S R	CK	
0 0	0	INVALID CONDITION
0 1	1	Pump OFF Q = 0
1 0	1	Pump ON Q = 1
1 1	0	No action

From the truth table,

$F_{S\text{-}R} = \sum(1,2)$ **(6)**

Plotting the Karmough map, and deriving the SOP expression for the synchronizing clock pulse (CK) generator, we have:



$$CK = \bar{S}R + \bar{S}R \quad \textbf{(7)}$$

The logic circuit of the synchronizing pulse generator derived from the above expression is shown in Figure 6.

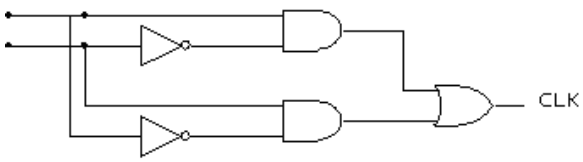


Figure 6: Logic Circuit of the Synchronizing Pulse Generator.

Figure 6 shows the circuit of an Ex-OR gate which can be represented by the symbol shown on Figure 7.

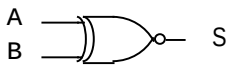


Figure 7: Ex-OR gate (Symbol).

The clocked S-R latch can be configured from the NOR and AND gates arrangement shown in Figure 8.

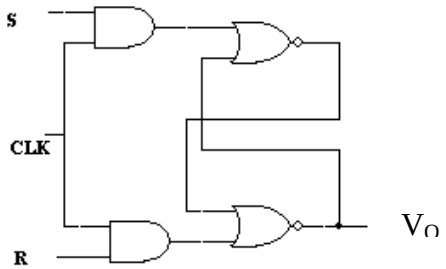


Figure 8: S-R Flip Flop with Clock Input.

Figure 9 is the logic control circuit of the WLE. It was generated by combining Figures 5a, 5b, 7 and 8.

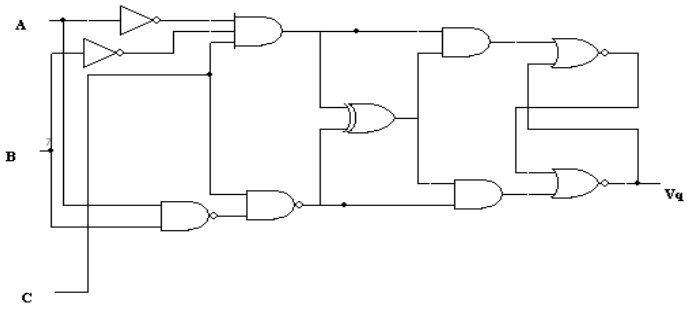


Figure 9: The logic Control Circuit of the WLE.

Inputs C, B, and A of the logic control circuit represent the outputs of - source sensor, reservoir full (high level) sensor, and reservoir virtually empty (low level) sensor respectively. Figure 10 shows the WLE sensor circuit.

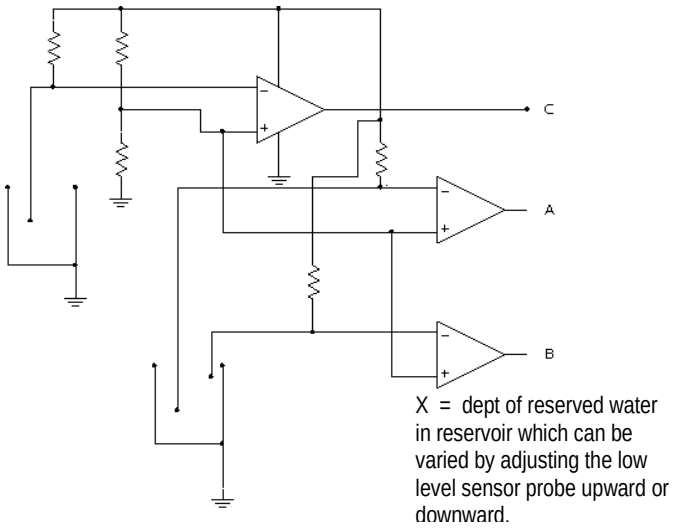


Figure 10: Circuit Diagram of WLE Sensor Locations.

Interfacing

The WLE logic control circuit can be electromechanically or optically interfaced to operate the mains water pump.

(a) Electromechanical Interface

Floyd, 2007 reported this electromechanical interface approach. This requires the use of a DC relay to connect the water pump. The current handling capacity of the relay contact must be more than twice the rating of the pump.

The relay internal resistance R_L determines the collector current of the drive transistor. The transistor is usually biased to operate as a switch and controlled by the Q output of the WLE logic control circuit. In cutoff condition, the emitter junction is not forward biased. This means that no base current flows into the transistor. Thus V_{CE} is approximately equal to V_{CC}.

$$V_{CE(cutoff)} \approx V_{CC} \quad \textbf{(8)}$$

Similarly in saturation, base-emitter junction is forward biased and there is enough base current to produce maximum collector current. In this state, $V_{CE(sat)}$ is negligibly small compared to V_{CC}. The collector current is:

$$I_{C(sat)} \approx \frac{Vcc}{R_L} \quad \textbf{(9)}$$

The minimum value of base current needed to produce saturation is:

$$I_{B(min)} \approx \frac{I_{C(sat)}}{\beta_{DC(max)}} \quad \textbf{(10)}$$

Where $\beta_{DC(max)}$ is the maximum limit of the DC current gain of the transistor.

$$\text{In saturation, } R_b = \frac{V_Q - V_{BE(sat)}}{I_\beta} \quad \textbf{(11)}$$

The diode (D) is needed to protect the transistor and some other circuit elements against the effect of the inductive kick of the relay.

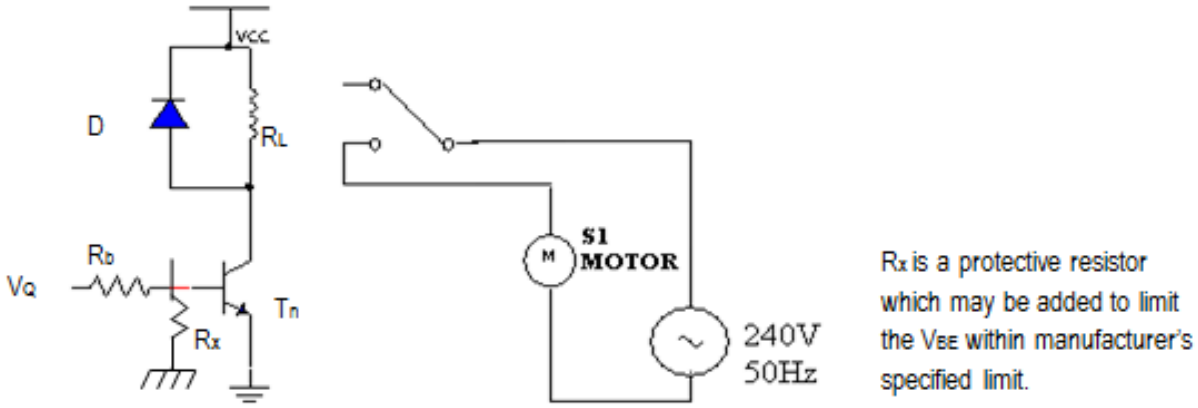


Figure 11: Interfacing Control Circuit Electromechanically to a Mains Operated Water Pump.

b) Optical Coupled Interface

Opto coupled triac may be used as an alternative to drive a triac of adequate current handling capacity to power the electric pump.

For very large capacity pump, zero crossing opto coupler is recommended to enable the pump start softly and limit any electromagnetic or radio frequency interference (NPES,1998)

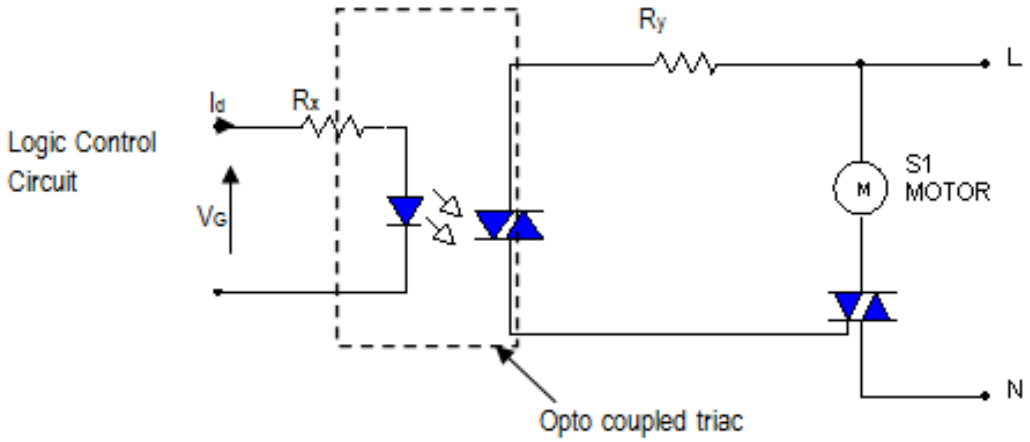


Figure 12: DC/AC Interface Using Opto Coupled Triac.

$R_x =$ $(V_Q - V_{Fd}) / I_d$ **(12)**

Typically V_{FD} = 2 volts and Id $\leq$ 10 milli amperes, R_y limits the current flowing through the opto coupled triac to a maximum value of 50 milliamperes.

Figure 13 is the comprehensive circuit of the water level equilibrator (WLE) while Figure 14 is the printed circuit board layout with the component footprints shown.

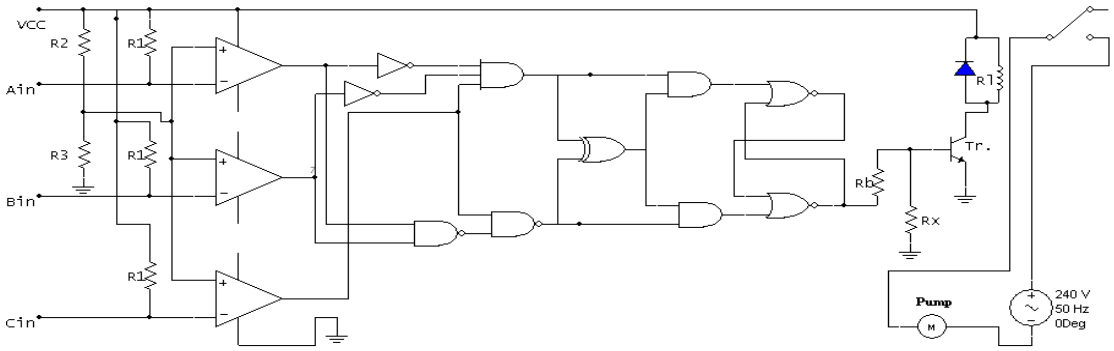


Figure 13: The Circuit of Water Level Equilibrator (WLE).

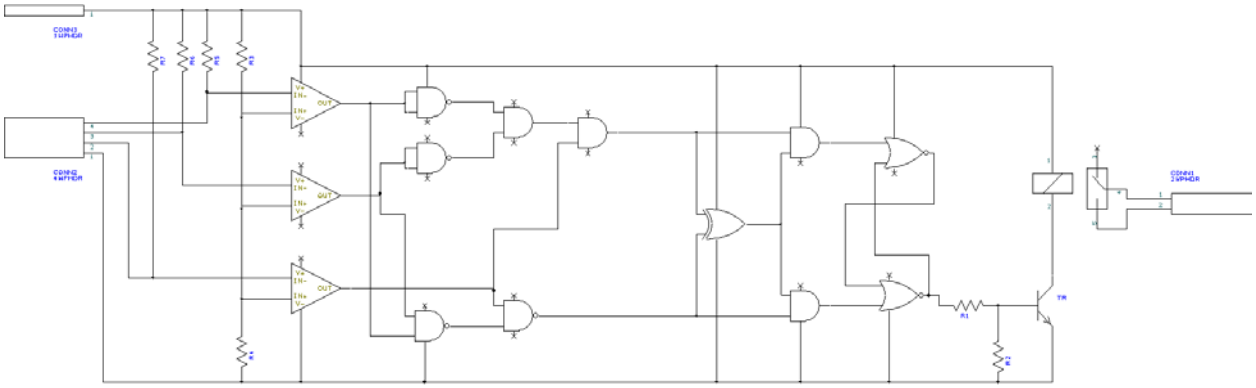


Figure 14: The Equivalent Circuit of Figure 13.

Implementing the circuit of Figure 13 will create many redundant gates and increase the circuit board size. Conversion of the unused NAND gates of the C-MOS integrated circuit package to INVERTER gates and its two 2-input AND gates to the 3-input equivalent as illustrated in Figure14, which limits any such wastes and redundancies. Figure 14 therefore, is the equivalent circuit of Figure13 but with minimal number of redundant gates and reduced circuit board size.

The schematic diagram of Figure 14 is drawn using the printed circuit board (PCB) Artist software version 1.3.3 and converted to PCB layout using the auto route option. The PCB layout is displayed in Figure15 while the design rule check result of the board is shown in Table 3.

Table 3: Design Rule Check Report

Report File : F:\Documents and Settings\TAE\Desktop\Design1 (PCB - Design Rule Check Report).txt
Report Written : Monday, October 31, 2011
Design Path : F:\Documents and Settings\TAE\Desktop\Design1.pcb
Design Title : Water Level Equilibrator (WLE)
Created : 10/31/2011 11:27:17 PM
Last Saved : 10/31/2011 11:27:29 PM
Editing Time : 2 min
Units : mil (precision 0)

Results
No errors found

Settings
Spacings

Tracks	Yes
Pads and Vias	Yes
Shapes	Yes
Text	Yes
Board	Yes
Drills	Yes
Components	No

Manufacturing

Min Drill Hole Size	Yes
Min Track Width	Yes
Min Annular Ring	Yes
Drill Breakout	Yes

Nets

Net Completion	Yes
Dangling Tracks	Yes
Net Track Length Differences	No

End Of Report.

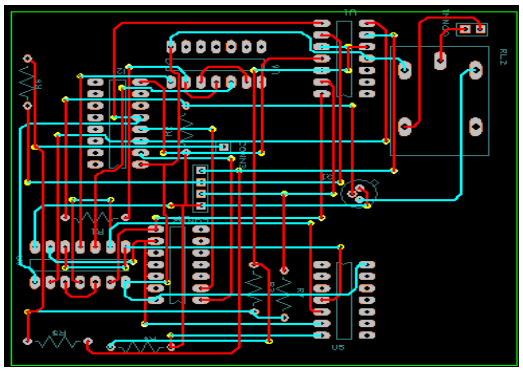


Figure 15: The PCB Layout of WLE.

CONCLUSION

Power supply is not considered a critical issue in this design because voltage tolerant components were considered. Also two choices of interface have been listed and considered-solid state and electromechanical interface. Every aspect of this design was not only subjected to simulation using NI multisim version 11 but was also physically wired up, coupled, installed and satisfactorily tested with a single phase 2HP 220volts mains pump.

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