Design, Simulation, and Testing of an Incremental Shaft Encoder for Measuring Angular Velocity of a Shaft.

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ABSTRACT

An incremental shaft encoder has been designed, simulated, and developed for measuring angular velocity of a shaft. The design was achieved using the following components; a disc of a plastic material with fifteen slots and mounted on the shaft of a DC motor. An opto-interrupt device (OID), an infrared light emitting diode and photo transistor, 555 timer, AND Gate, D-type flip flop, encoder, decoder, differentiator (logic control), and display. A bubble resolver was also added to the circuit to eliminate ±1 counting error that is inherent in most digital devices. The incremental shaft encoder designed and developed was able to measure a maximum speed of 2500rpm and a corresponding frequency of 625Hz of a 12V DC motor after proper calibration and testing in the laboratory. The circuit designed and developed is a prototype of an industrial incremental shaft encoder.

(Keywords: eliminate, counting error, simulation, measurement, configure, OID, opto-interrupt device)

INTRODUCTION

Digital electronics instruments are preferred to analogue instruments these days because digital electronics instruments enhance accuracy of measurements, minimize loading effects, and reduce electrical noise (Ali, 2006).

An incremental shaft encoder is used generally to monitor the speed of motors or generator shafts. This research utilizes a practical shaft encoder using opto-interrupt device (OID). An OID is a device that combines infrared light emitting diode (LED) and photo transistor in close proximity. Equally spaced slots on the plastic disc that allow light from the infrared LED to trigger the base of the photo transistor while the photo transistor generate 15 pulses for one revolution of the shaft. The circuit can be used to monitor the change in angular position of a motor shaft or its speed. For regularly spaced slots, the interval between any slots is giving by 360/n, where n is the number of pulses (Ali, 2006 and Colin, 2003). A count of total number of pulses thus relates the angular displacement of the shaft. The simulation was done by Electronic Work Bench (EWB) professional version. This design, simulation and construction were carried out in the department of pure and applied Physics Adamawa State University, Mubi Nigeria.

The time base generates a gating pulse of constant time duration of 1s which serves as the means of opening and closing the gates for trains of the pulses at the output of the comparator to pass through the AND gate. These trains of pulses are received by the n-binary counters processed and display the data. The purpose of this work is to design a machine that could display in digit the angular speed of any rotating shaft.

COMPONENTS/DESIGN PROCEDURES

The design consists of the following stages; disc design, D flip flop, time base, control logics and Binary Coded Decimals (BCD).

Disc Design

The disc was cut in a circular form at a radius of 2.5cm and fixed to the shaft whose angular velocity is to be determined. The slots were drilled at regular interval of 24^0 using Equation (1) as shown in Figure 1:

$$Slots\ interval = \frac{360}{n} \quad \textbf{(1)}$$

Where n is the number of slots in the disc.

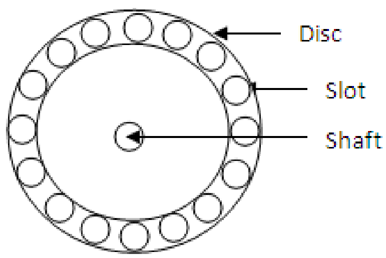

Figure 1: Slotted Disc.

D type flip-flop (Bubble Resolver)

The bubble resolver is use in the design as a synchronizer its function is to remove or eliminate the ±1 counting error that is inherent in opto-interrupt circuit. The output of the AND gate does not come ON until the first clock arrives at the clock point of the D flip-flop with the time base gating pulse, it opens when both pulses are HIGH and continuous until gating pulse from time base goes away (LOW), thus locks the measured interval (gating pulse) to the event signal pulse being measured and eliminate the bubble. The AND gate receive the output of the D flip flop (Morris, 2002). During the simulation, a clock was connected to the infrared terminal which gives pulses similar to the behavior of the slotted shaft. When the output of the opto-device was fed to the D flip flop, its clock input was triggered with a 300 Hz clock from the EWB library. The output of the AND Gate was fed to an oscilloscope and the output waveform is shown in Figure 2.

Time Base

The timer used in this design is configured as a stable multi vibrator that generates a gating pulse of constant time duration (ΔT) of 4s which serves as the opening and closing of the logic gate. The period when the gating pulse is high is given by (Robert, 2004).

$$T_1 = \ln 2(R_1 + R_2)C_1 \quad \textbf{(2)}$$

While the period when the gating pulse is low is:

$$T_2 = \ln 2R_2C_1 \quad \textbf{(3)}$$

Then the total period of the trains of the pulses to be counted is given by (Ronald, 2004).

$$T = \ln 2(R_1 + 2R_2)C_1 \quad \textbf{(4)}$$

The frequency of operation of the shaft is given by (Onuu et al, 2006 and Philips, 2009).

$$f_1 = \frac{1}{T} \quad \textbf{(5)}$$

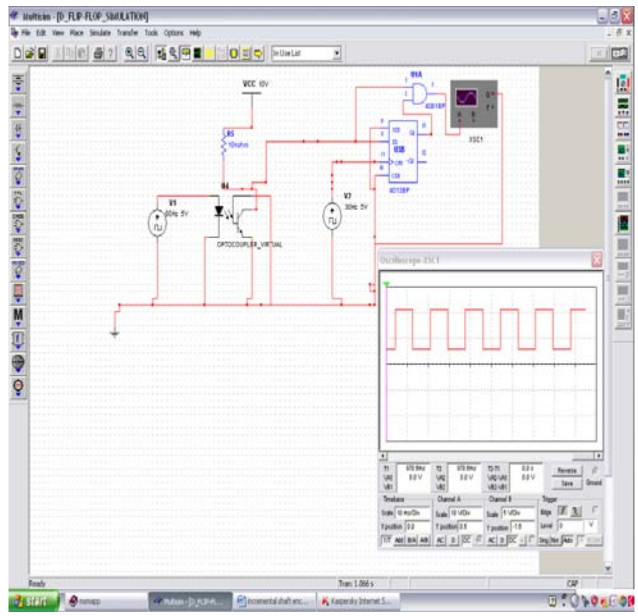

Figure 2: D Flip-Flop Circuit and Simulated Waveform.

Since the period for which the pulse goes HIGH is 4s, the period for it to go LOW is chosen as 0.15s, choosing C_1 to be 0.1uf and R_2 was determine using (3) to be 1K to the nearest preferred value. Substituting the values in (2) R_1 yields 1k. Using (4) in (5), the frequency of oscillation of the shaft was obtained as 0.24Hz. The simulated circuit of the time base is shown in Figure 3.

Control Logic (Differentiator)

The function of the differentiator is to reset the counter. The frequency needed to reset the counter is given by (Efedua, 2004). While the frequency was obtained as

$$f_2 = \frac{1}{2\pi R_6 C_3} \tag{6}$$

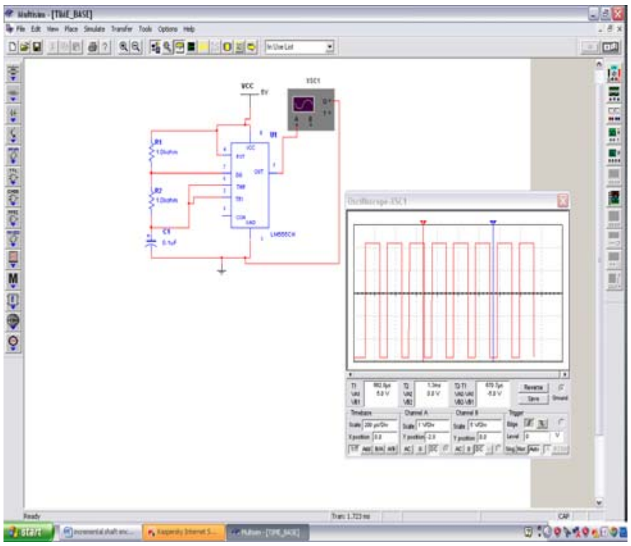

Figure 3: Time Base (555 Timer) Circuit and Simulated Waveform.

Binary Coded decimal Counter (BCD)/Seven Segment Decoder

Figure 4 shows the complete circuit diagram of the CD4510 binary Coded decimals counter and CD4511 BCD to seven segment decoder was configured to a seven segment light emitting diode. During the simulation, 1 KHz clock pulse was fed to the clock input of the BCD counter to confirm its operation.

Power Supply

The power supply used in this design incorporate two integrated circuits regulator, which have fixe voltage regulators producing +5V and +12V . The transformer is a 220VAC, 15V output. The rectifier is a full wave bridge, which makes use of four rectifier diodes of required rating. The output of the AC voltage is filtered by 220uF, 50V capacitor. The 12V regulator used was KA7812 and the 5V regulator was KA7805.1uf in parallel with 1nF ceramic capacitor was used at the output to further remove any ripple.

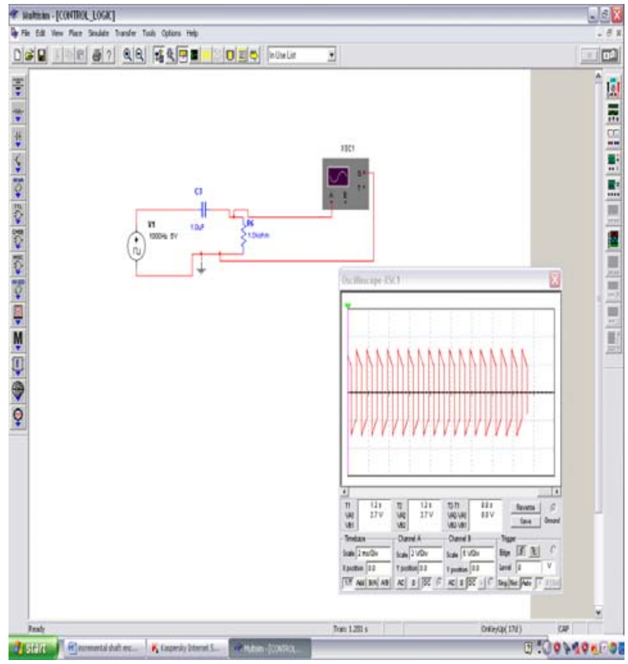

Figure 4: Simulated Circuit of Control Logic.

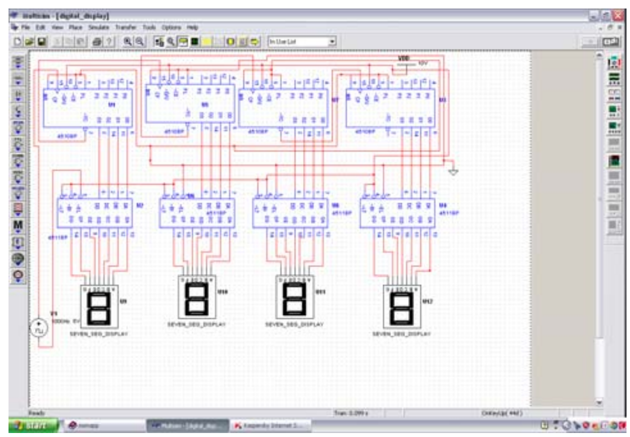

Figure 5: BCD/ BCD to Seven Segment Decoder and its Digital Display.

Construction Details

The construction of the circuit did not commence until the circuit was tested on breadboard and found to be working well. The circuit was tested using three breadboards, the counter-decoder unit was mounted on the breadboard, and a 555 timer was configured as an oscillator which was used to check the working of the counter and the decoders.

After the design and simulation, the disc was cut to a circular shape with a diameter of 80mm, 15 slots were marked out with compass and protractor at an angular spacing of 24^0. The slots were drilled with the aid of a 4mm drill bit using drilling machine.

The next stage was the optical interruption section which was tested on a breadboard together with the slotted disc. The pulses generated were monitored by a light emitting diode before transferring to a Vero-board.

The timer stage was next constructed whose output was tested with two light emitting diodes connected between the supply to the output and the output to the ground respectively to confirm it bistable mode of operation.

The power supply, the time base, bubble resolver, control units were constructed on a single Vero-board with the seven segment displays constructed on another different Vero-board.

RESULTS, ANALYSIS, TESTING AND DISCUSS

Table 1 shows the result obtained after the design, construction, simulation, and testing of the general circuit.

Table 1: Speed in (RPM) and the Corresponding Frequencies (Hz).

Test	Speed (ω) in rpm	Frequency (f) in Hz
1	100	16
2	200	32
3	300	48
4	400	64
5	500	80
6	600	96
7	700	112
8	800	128
9	900	144
10	1000	160

When the shaft starts rotating, the slots act as a switch interrupting the signal to the photo transistor causing its output to generate pulses. The train of pulses generated depends on the speed (ω_{rpm}) of the rotating disc which is given by:

$$\omega_{rpm} = \frac{M_{ppm}}{15} \tag{7}$$

Or its revolution per second or frequency in (Hz)

$$\omega_{rps} = 4M_{pps} \tag{8}$$

Where $M(rpm)$ is the number of pulses generated per minutes? If the pulses generated in a time $t_{(min)}$ is say Y, then,

$$M_{ppm} = \frac{Y_{pulse}}{t_{\min}} \tag{9}$$

If the pulses are recoded at an interval of 1min for say 5min. a graph of Y (angular velocity) against f (frequency) gives a straight line whose slope is given:

$$M_{ppm} = \frac{\Delta Y_{pulse}}{\Delta t_{\min}} \tag{10}$$

Equation (6) presents the gradient (M) = 4 rpm/Hz of the straight line graph in Figure 6, which described the relationship between the angular velocity (rpm) and the frequency (Hz).

Figure 7, presents the simulated results during testing in the laboratory before any adjustment. The time base unit was calibrated to give precisely gating pulse of 4s, the signal generated was set to a frequency of 16Hz (square wave) and the gating pulse was adjusted until it gave a reading of 100rpm, to further confirm the accuracy of the calibration, the frequency was increase to 140Hz and the shaft encoder gave a reading of 1250rpm as depicted in Figure 8, then some certain test were carried out at an interval of 16Hz as shown in Table 1 Which described number of pulses generated per minute. As the frequency increases the speed also increases.

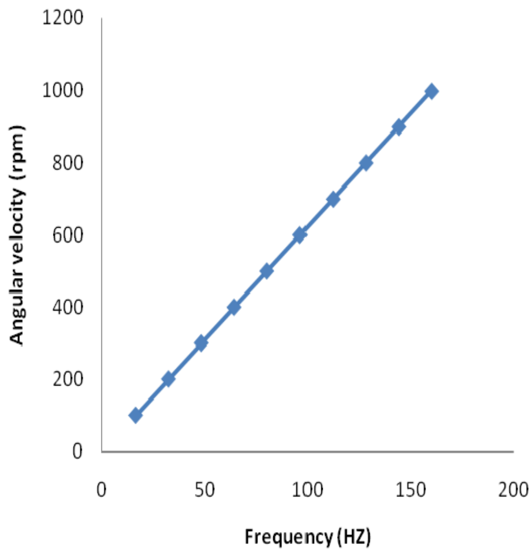

Figure 6: Angular Velocity (RPM) against Frequency (Hz).

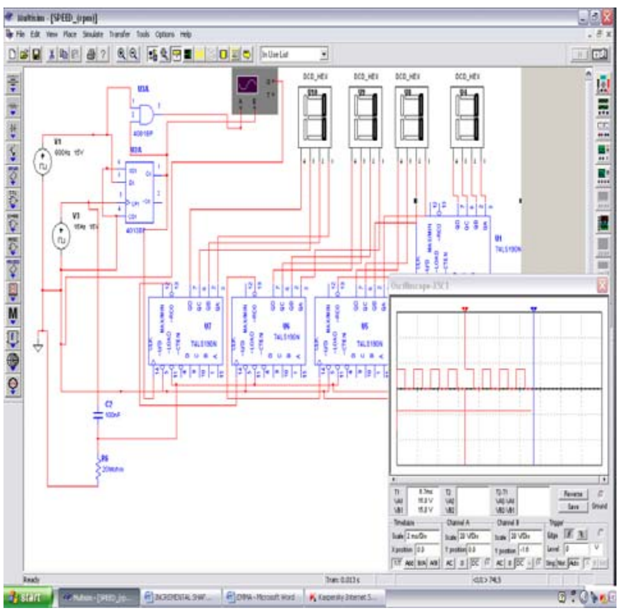

Figure 7: Display of Angular Velocity before Adjustment.

Figure 3, described the operation of the time base, the output V_0 the capacitor C_1 is charged by current flowing through R_7 and R_8. The threshold and trigger inputs monitor the capacitor (C_1) voltage and its reaches 2/3 V_0 (Threshold Voltage) the output becomes LOW and the discharge pin is connected to 0. The C_1 now discharges with the current flowing through R_8 into the discharge pin. When the voltage fall to 1/3V_0 (Trigger Voltage) the output becomes HIGH again and the discharge pin is disconnected, allowing C_1 to start charging again. This cycle repeats continuously unless the RESET input is connected to 0V which forces the output low while the reset is 0V.

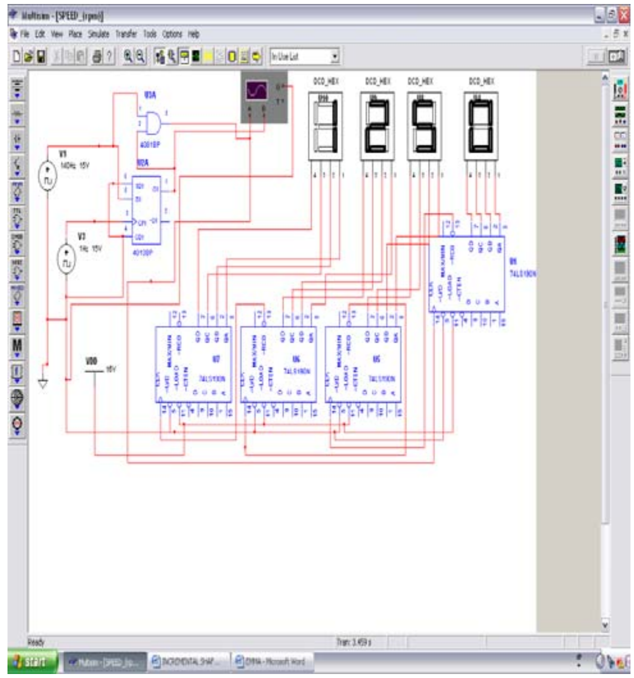

Figure 8: Display of Angular Velocity after Adjustment.

Figure 4, explains how the D flip flop operates, the D flip flop tracks the input, making transitions with the match those of the input D. The D flip flop has only input if there is a HIGH on the D input when the clock pulse is applied, the flip flop SETs and stores 1 as HIGH. If there is a Low on the D input when the clock pulse is applied, the flip-flop RESETs and stores a 0 as LOW.

Figure 5 described the operation of the control logic circuit. If we apply a constantly charging signal such as a square wave type signal to the input of the control logic the resultant output signal will be charged and whose final shape is strictly dependent upon the value of C_3 and R_6.

Most of the previous circuits of the shaft encoder in existence were deficient in the following areas; poor sensitivity or low efficiency, digital counting error of plus or minus 1. This work eliminates the deficiency and improved the efficiency of the circuit of the incremental shaft encoder. This design used the professional version of Electronic Work Bench (EWB) software throughout because mixing it up with other soft wares could cause poor performance and low efficiency because it will definitely requires an interface which would be another design problem to check intensively. Secondly the BCD design used only TTL instead of the ECL and the CMOS logic families because of incompatibility with the TTL circuitry.

CONCLUSION

The design of the Incremental Shaft encoder for measuring angular velocity of the shaft using a 12V DC motor was achieved despite a lot of assumptions and approximations, the design improved the efficiency of the existing circuit in the market by replacing the comparator with bubble resolver an AND Gate to eliminate ±1 error that is inherent in most digital systems. This model is capable of measuring angular velocity of shaft although is hardly used by Nigerian industry except in areas where they come indispensible; if this is develop by our local industries in no distant time incremental shaft encoder will be available in the market as other digital instruments.

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