An FPGA Based Hardware Algorithm Implementation for Cascaded Multilevel Inverters.

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ABSTRACT

In recent years, Field Programmable Gate Arrays (FPGAs) have become key components in implementing high performance digital signal processing (DSP) systems, especially in the areas of digital communications, networking, video, and imaging, but its potential is not fully utilized in the area of power control and conversions. FPGA far exceeds that of a microprocessor or DSP processor running at clock rates two to ten times that of the FPGA. Coupled with a capability for implementing highly parallel arithmetic architectures, this makes the FPGA ideally suited for creating high-performance custom data path processors for tasks such as digital filtering, fast Fourier transforms, and forward error correction.

In this paper a XILINX FPGA based multilevel PWM three phase inverter was constructed by adding bidirectional switches to the conventional bridge topology. The inverter can produce three and five different output voltage levels across the load. FPGA is used as a SVPWM generator to apply the appropriate signals to inverter switches. In addition to XILINX FPGA, Matlab/Simulink®, system generator software was used for simulation and verification of the proposed circuit before implementation, simulation, and experimental results show that both are in close agreement. The present PWM signal generation scheme can be used for any multilevel inverter configuration.

(Keywords: cascaded multilevel inverter, FPGA, space vector pulse width modulation, THD)

INTRODUCTION

Multilevel converters offer many benefits for higher-power applications. In particular, these include an ability to synthesize voltage waveforms with lower harmonic content than two level converters and operation at higher DC voltages using series connected semiconductor switches. While many different multilevel converter topologies have been proposed, the two most common topologies are the Cascaded Inverter and its derivatives [1][2], and the Diode Clamped inverter [3]. Figure 1 shows topology for five level configuration of a Cascaded Multi Level Inverter. The two most popular control strategies for these multilevel inverter topologies are Carrier [4] and Space Vector (SVM)[6], [7] modulation.

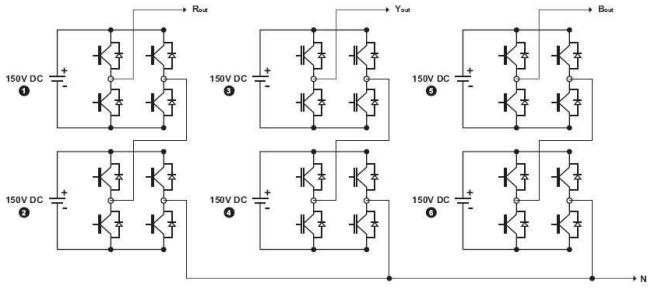

Figure 1: Five Level Cascaded Multilevel Inverter.

A Field Programmable Gate Array (FPGA), is a type of logic chip that can be programmed. An FPGA is similar to a PLD, but whereas PLDs are generally limited to hundreds of gates, FPGAs support thousands of gates.

They are especially popular for prototyping integrated circuit designs. Once the design is set, hardwired chips are produced for faster performance. The inherent parallelism of the logic resources on an FPGA allows for considerable computational throughput even at a low MHz clock rates. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. This has driven a new type of processing called reconfigurable computing, where time intensive tasks are offloaded from software to FPGAs [5].

SVM involves switching between the three nearest space vectors from the available states of an inverter. Several approaches have been presented to show how these space vectors can be selected for particular operating conditions [8]. For applications such as ac motor drives, it is desirable to minimize the harmonics and inter harmonics voltage to prevent premature bearing failure and reduce EMI levels. Several modulation variations that achieve this result have been reported SVM scheme. The advantages of SVM [8][11] are as follows:

- Line to line voltage amplitude can be as high as VDC. Thus 100% VDC utilization is possible in the linear operating region.

- In the linear operating range, modulation index range is 0.0 to 1.0 in the sine PWM, where as in the SVM, it is 0 to 0.866. Line to line voltage amplitude is 15% more in the SVM with the modulation index=0.866, compared to the SPWM with modulation Index = 1. Hence it has the better usage of the modulation index depth.

- With the increased output voltage, the user can design the motor control system with reduced current rating, keeping the horse power rating at the same level. The reduced current helps to reduce the inherent conduction loss of the VSI.

- Only one reference space vector is controlled to generate the three phase sine waves.

- Implementation of SVM switching rules gives less THD and less switching loss.

- Flexibility to select inactive states and their distribution in switching time periods gives two degrees of freedom.

- As a reference space vector is a two dimensional quantity, it is feasible to implement more advanced vector control using SVM.

Figure 2 shows the space vector states for the proposed five level cascaded inverter.

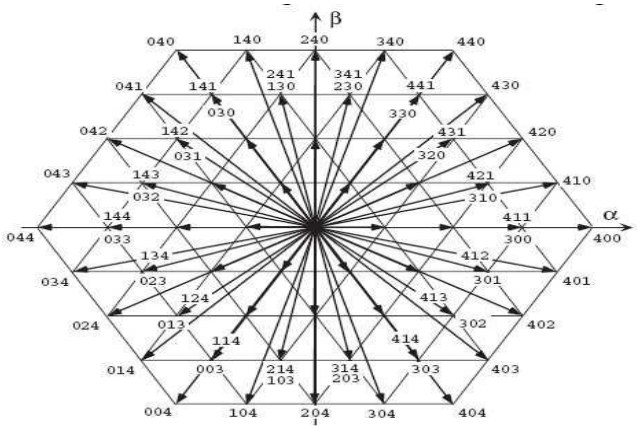

Figure 2: Space Vector States for 5 Level Inverter.

FPGA IMPLEMENTATION

The FPGAs have become key components in implementing high performance digital signal processing (DSP) systems [5]. The logic fabric of today's FPGAs consists not only of lookup tables, registers, multiplexers, distributed and block memory, but also dedicated circuitry for fast adders, multipliers, and I/O processing (e.g., giga-bit I/O). The memory bandwidth of a modern FPGA far exceeds that of a microprocessor or DSP processor running at clock rates two to ten times that of the FPGA. Coupled with a capability for implementing highly parallel arithmetic architectures, this makes the FPGA ideally suited for creating high-performance custom data path processors for tasks such as digital filtering, fast Fourier transforms, and forward error correction.

The processors and DSPs, even when running at GHz clock rates, are increasingly used for relatively low MIPs packet level processing, with the chip and symbol rate processing being implemented in the FPGAs and ASICs. The fluidity of emerging standards often makes FPGAs, which can be reprogrammed in the field, better suited than ASICs. Though VHDL provides

many high level abstractions and language constructs for simulation, its synthesizable subset is far too restrictive for system design. System Generator is a software tool for modeling and designing FPGA-based DSP systems in Simulink®. The tool presents a high level abstract view of a DSP system, yet nevertheless automatically maps the system to a faithful hardware implementation. The most significant is that System Generator provides these services without substantially compromising either the quality of the abstract view or the performance of the hardware implementation.

System Generator

Simulink® provides a powerful high level modeling environment for DSP systems, and consequently is ideally used for algorithm development and verification. System Generator maintains an abstraction level very much in keeping with the traditional Simulink® block sets, but at the same time automatically translates designs into hardware implementations that are faithful, synthesizable, and efficient [12]. The implementation is faithful in that the system model and hardware implementation are bitidentical and cycleidentical at ample times defined in Simulink®.

The implementation is made efficient through the instantiation of intellectual property (IP) blocks that provide a range of functionality from arithmetic operations to complex DSP functions [12]. These IP blocks have been carefully designed to run at high speed and to be area efficient. In System Generator, the capabilities of IP blocks have been extended transparently and automatically to fit gracefully into a system level framework. For example, although the underlying IP blocks operate on unsigned integers, System Generator allows signed and unsigned fixed point numbers to be used, including saturation arithmetic and rounding. User-defined IP blocks can be incorporated into a System Generator model as black boxes which will be embedded by the tool into the HDL implementation of the design.

MODELING WITH SYSTEM GENERATOR

Before developing the hardware circuit for power, control and isolation circuit based on the FPGA, the entire system is generated with the aid of simulation package Simulink®/System Generator for FPGA in order to verify the pulses and the patterns of the output pulses.

The creation of a DSP design begins with a mathematical description of the operations needed and concludes with a hardware realization of the algorithm [12]. The hardware implementation is rarely faithful to the original functional description instead it is faithful enough. The challenge is to make the hardware area and speed efficient while still producing acceptable results. In a typical design flow, a flow supported by System Generator the following steps occur:

1. Describe the algorithm in mathematical terms,
2. Realize the algorithm in the design environment, initially using double precision,
3. Trim double precision arithmetic down to fixed point,
4. Translate the design into efficient hardware.

Step 4 is error prone because it can be difficult to guarantee the hardware implements the design faithfully. System Generator eliminates this concern by automatically generating a faithful hardware implementation.

SIMULATION BLOCKS AND RESULTS

The proposed algorithm is generated in front end with the aid of system generator editor, the SVM blocks and the associated blocks for individual phases are interconnected and the sampling frequency is set to 5kHz. The entire system is shown in Figure 3.

The generated output pulses from the main SVM blocks are converted in to eight numbers which is required to drive the devices in to ON state with the aid of pulse converter blocks as shown in Figure 4. The pulse for the individual switches from 1 to 4 is as shown in the Figure 5 and the pulses for the switches from 5 to 8 is as shown in the Figure 6, for the remaining switches these pulses are inverted suitably to the same group and supplied. The line to line and phase voltages are as shown in Figure 7 and Figure 8, respectively.

The switching patterns adopted are applied at the cascaded multilevel inverter switches to generate five or three output voltage levels at different modulation indexes.

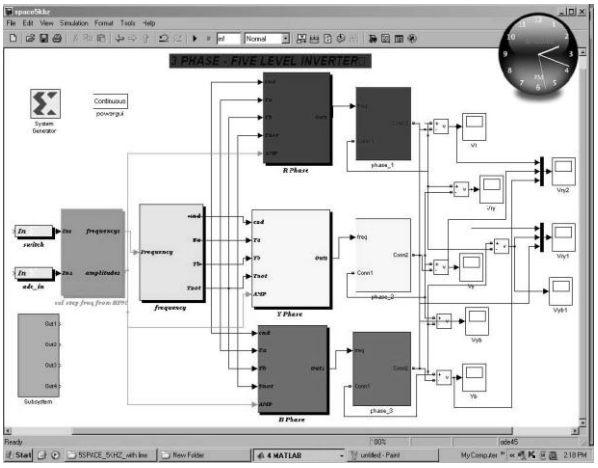

Figure 3: Block Diagram for Generation of Firing Pulses for Three Phase, Five Level Cascaded Multilevel Inverter.

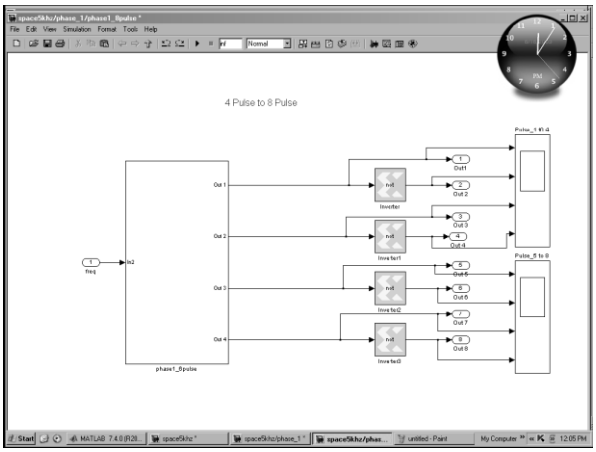

Figure 4: Pulse Converter–Four to Eight Pulse Conversion.

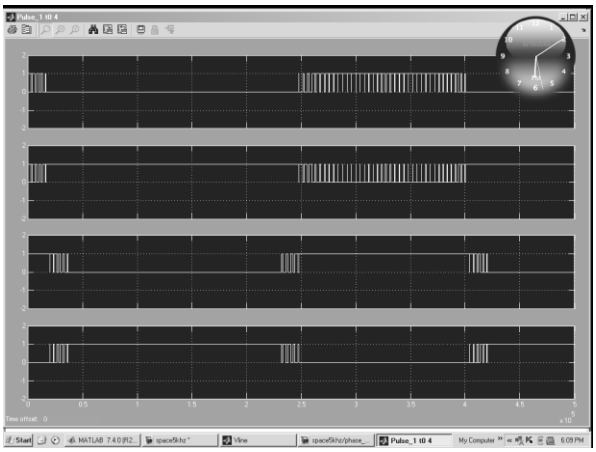

Figure 5: Pulses for the Cascaded Multilevel Inverter Switches 1 to 4.

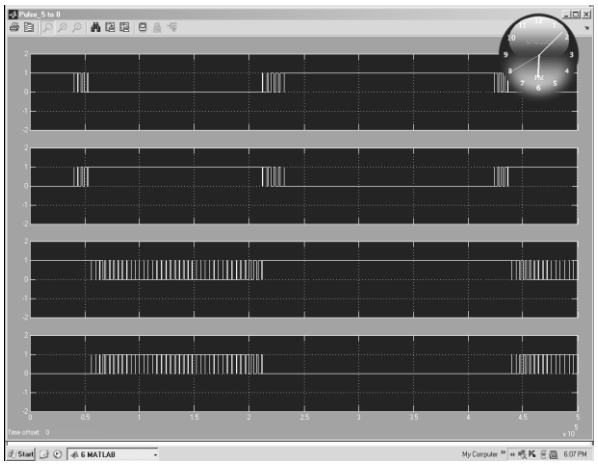

Figure 6: Pulses for the Cascaded Multilevel Inverter Switches 5 to 8.

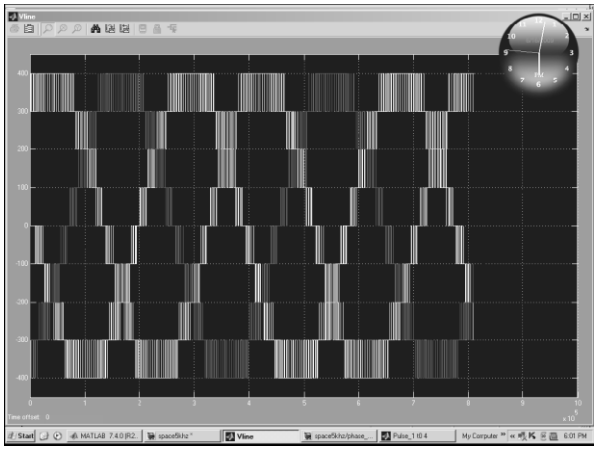

Figure 7: Output Line to Line Voltage.

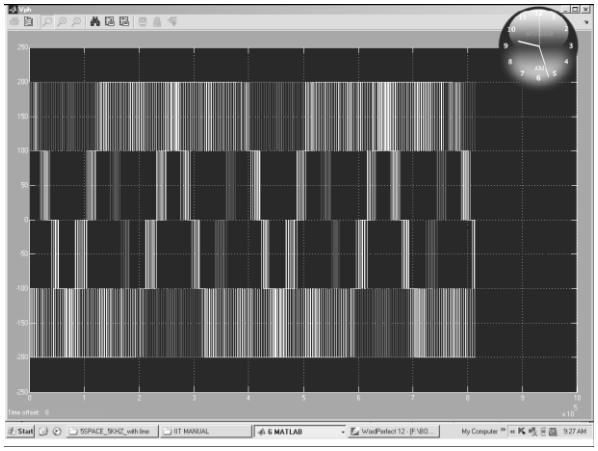

Figure 8: Output Phase Voltages.

XILINX FPGA enables to make easy, fast and flexible design and implementation. The THD profile for the simulation system is as shown in Figure 9, which shows the results are well within the specified limits of IEEE standards. The experimental and simulated results are show satisfactory results in term of total harmonic distortion and output voltage and current waveform shapes

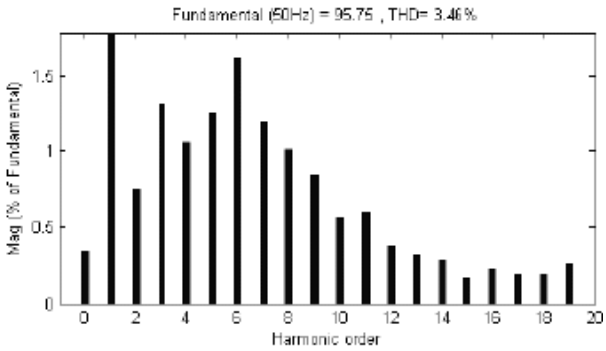

Figure 9: THD Profile of the Simulated Output.

CONCLUSIONS

This paper proposes a FPGA based new PWM switching strategy for the cascaded multilevel inverter. This scheme employs a Space Vector Modulation Technique. The main advantage of this technique is the ability to generate PWM waveform generation in real time using very simple algorithm in the XILINX processor. This reduces the computation time, required to determine the switching times for inverter legs, memory requirement of the digital processors making the algorithm suitable for real time implementation. Furthermore it also results in higher fundamental component magnitude. This paper carried out the simulation on a five level CMI to justify the merits of the proposed scheme. A low cost FPGA based three phase five level CMI test-rig is also constructed to verify the simulation results.

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