A Compound Compensation Using DFACTS and Switch Based Fault Current Limiter (SFCL).

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ABSTRACT

Power quality improvement has become a very important topic in power systems over the past several decades. Custom power devices (DFACT) are a kind of Flexible AC Transmission Systems (FACTS) devices which are used for power quality enhancement in distribution networks. The cost of DFACTs will be increased with growth in their size and required power rating. This paper proposed a structure based on using the combination of a new switch based fault current limiter (SFCL) and DFACTSs to decrease the required power rating and size of compensator device. This method can be used to reduce the cost of both series and shunt compensators. The proposed technique is implemented on a test system with suitable results.

(Keywords: custom power device, shunt compensation, series compensation, switch based fault current limiter, SFCL, power quality)

INTRODUCTION

Due to the rapid rate of increasing loads and the comprehensive use of nonlinear loads in power systems, power quality has become a very important topic especially after power system restructuring. Any power problem manifested in voltage, current, or frequency deviations that results in failure or mis-operation of customer equipment can be defined as power quality problem [1].

Two important power quality problems are voltage sag and harmonic distortion. According to IEEE standard 1159-1995, voltage sag is voltage drop from 10% to 90% with 10ms to several seconds [1]-[2]. Voltage sag can damage customers, especially critical loads which need uninterruptable voltage with high quality. Several problems can cause voltage sag. One of the most important of them is the overhead radial distribution lines [3]. When a fault occurs, the voltage sag is proportional to a short circuit current [3]. Therefore, the devices which are able to limit the short circuit current can be used to mitigate voltage sag.

Harmonics are sinusoidal voltages or currents which have different frequencies, more than frequency of supply system, which are not desirable for the power systems [1]. A waveform can be disintegrated to sum of fundamental frequency and harmonics. Total harmonic distortion (THD) is chosen as a criterion to evaluate the harmonic distortion. THD is defined with dividing the square-root of the sum of squares of the amplitudes of all harmonics by magnitude of the fundamental frequency [1].

The system operators use several types of equipment and methods to improve power quality in the power systems. Custom power devices (DFACTS) are one of the best types of equipment which can be used to enhance power quality in the distribution networks. Series, shunt, and series-shunt are three kinds of compensation method which can be implemented by DFACTSs. The series compensators are able to adjust voltage drop and harmonic of voltage and also control power flow by governing the series injected voltage [4]-[6]. By controlling the injected current in the shunt compensators, the system operator can compensate the reactive power and harmonics of the current for the nonlinear loads [7]-[9]. Series-shunt compensators are a combination of both series and shunt compensators which include all of their ability for power quality improvement [10]-[12].

The cost of DFACTSs depends on their rate of required power and size, with price increasing

along with the power rating. Therefore, if the operator is to be able to use the DFACTS with a lower power rating for improving power quality, it can reduce the investment cost for system compensation.

This paper proposes a method for reducing the required power rating and size of custom power devices which are used for compensating in the distribution networks. The proposed method is based on using the combination of a new switch based fault current limiter (SFCL) and shunt or series compensator (depending on the kind of compensation which the system requires). By using this method the amount of required series voltage or shunt current which the compensator should inject to the system to improve power quality will be reduced. Therefore, using of the DFACTS with lower power rating and consequently lower cost is possible.

BASICE CONCEPT OF COMPENSATION

Shunt Compensation

Figure 1 shows the schematic of the shunt compensation for improving the system power quality. By controlling the injected current, the inverter can compensate the reactive power and harmonic of the current for the nonlinear loads.

Equation (1) can be used to determine the RMS value of injected power of shunt inverter [13]:

$$I_{inject} = (\sqrt{1 - PF^2 + THD^2})\, I_{load} \qquad \textbf{(1)}$$

Where, I_{load} = The current of load
PF = The worst amount of load power factor
THD = Total harmonic distortion of current of the load

The rate of voltage of the shunt inverter is equal to the rate of voltage of the load. Therefore, the maximum required Volte-Ampere (VA) for the compensator can be calculated by multiplying its rate of the voltage and maximum injected current.

By adding switches between the power supply and shunt inverter, the shunt device can be used as an uninterruptable power supply (UPS) for the load during a short time voltage interruption. For this action, the shunt device needs an energy storage unit such as battery or SMES. The size of energy storage unit can be computed by multiplying power of the load and maximum period of the voltage interruption [13].

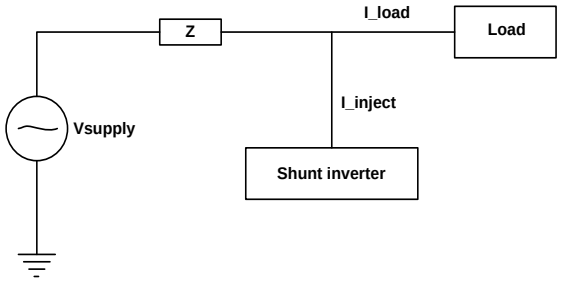


Figure 1: Shunt Inverter scheme for Improving Power Quality.

Series Compensation

This kind of compensation is able to adjust voltage drop and harmonic of voltage and also control power flow by governing the series injected voltage. Figure 2 depicts the scheme of series compensation.

Equation (2) can be used to define the injected voltage of series compensator [13]:

$$V_{inject} = (\sqrt{(\frac{\%V_{dip}}{100})^2 + THD^2})\, V_{\sup ply} \qquad \textbf{(2)}$$

Where, V_{supply} = The voltage of load
$\%V_{dip}$ = The percentage of voltage dip
THD = Total harmonic distortion of voltage of the load

To determine the stored energy for compensating voltage drop, magnitude of the voltage drop should be multiplied to current of the load and period of the voltage drop. For the UPS mode, the rate of compensation should be equal to the rate of full load. The size of energy storage unit can be calculated by multiplying the power of load to period of the interruption [13].

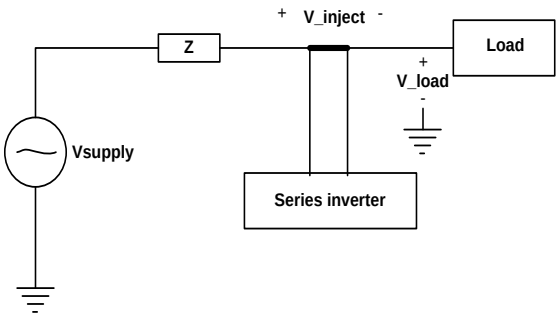


Figure 2: Series Inverter scheme for Improving Power Quality.

SWITCH BASED FAULT CURRENT LIMITER (SFCL)

Several researchers in the literature have used different structures of fault current limiter (FCL) for power quality enhancement [3] and [14]-[15]. In this section a simple structure which is based on using solid state transfer switch (SSTS) and fault current limiter (FCL) is proposed to limit the current of fault and improve power quality.

Solid State Transfer Switch (SSTS)

The SSTS is a very high-speed switch which is based on power electronic devices and is able to transfer the electrical load from one AC power source to another within a few milliseconds [14]. A general scheme of the SSTS is shown in Figure 3.

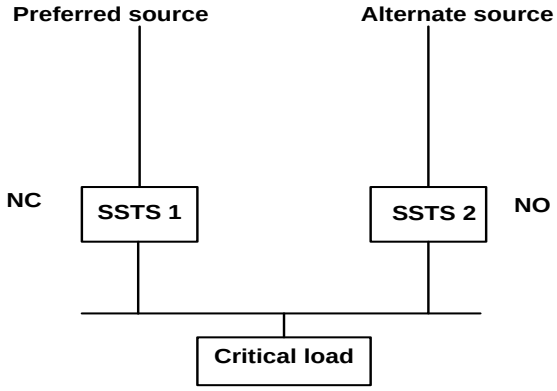


Figure 3: Solid State Transfer Switch (SSTS).

The SSTS consists of two AC thyristor switches and has two operating modes: ON-state and OFF-state. In the ON-state, the SSTS works in the low impedance forward conduction vice versa in the OFF-state which an open circuit with infinite impedance takes place. During normal condition SSTS1 works in ON-state and SSTS2 is OFF. On the detection of a fault in the normal feeder, the load should be fed by the backup feeder, therefore in this condition SSTS2 is ON and SSTS1 is OFF.

Principle Concept of Fault Current Limiter (FCL)

The FCL is a kind of custom power device which has been traditionally used for the limitation of large fault currents due to the extensive interconnection of power systems. Figure 4 illustrates the basic concept of current limitation. Consider Z_2 is very larger than Z_1 [14]:

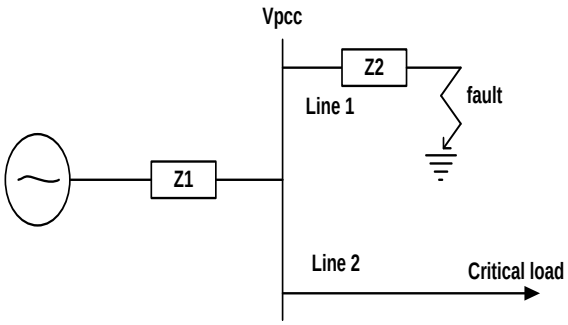


Figure 4: Critical Load Protected with FCL.

$$V_{pcc} = \frac{Z_2}{Z_1 + Z_2} V_{pre\_fault} \quad \textbf{(3)}$$

$$Z_1 + Z_2 \approx Z_2 \quad \textbf{(4)}$$

therefore:

$$V_{pcc} = V_{pre\_fault} \quad \textbf{(5)}$$

The FCL is able to limit the current of fault with large impedance. On the other hand, with paying attention to Equations (3) to (5), by selecting the very large impedance for FCL, this device can mitigate voltage sag. Therefore, the voltage of point of common coupling (Vpcc) will be approximately equal before and after fault condition.

Proposed Switch Based Fault Current Limiter (SFCL)

As previously mentioned, if Z_2 is much larger than Z_1, the FCL will be able to mitigate voltage sag. On the other hand, because of the large impedance of FCL (Z_2), if the electrical power is forced to pass through the FCL before the fault, it may cause electrical power loss and voltage sag at the loads which are placed after the FCL.

Some papers proposed a structure for an FCL with the series capacitor to control the impedance of FCL and keep it very low before the fault for preventing the mentioned effect [14]. But the series capacitor may cause bad effects on powers systems such as sub synchronous resonance (SSR). Therefore, it is better that before the fault occurrence, the FCL works at the OFF-state with very low impedance and if a fault occurs, the FCL switches to the ON-state with very high impedance to limit the current of fault and mitigate voltage sag.

A switch based fault current limiter (SFCL) which is based on using combination of FCL and high speed SSTS is proposed in this section. Figure 5 depicts scheme of the proposed SFCL. In this pattern, during normal condition, SSTS1 is at ON-state and SSTS2 is at OFF-state, therefore the FCL is off and electrical power passes through the normal line which has very low impedance. On the detection of a fault, the state of switches changes very fast and electrical power should pass through the FCL which has large impedance. Therefore, the proposed SFCL is able to limit the current of fault and mitigate the voltage sag without any bad effect on the system before the fault occurrence.

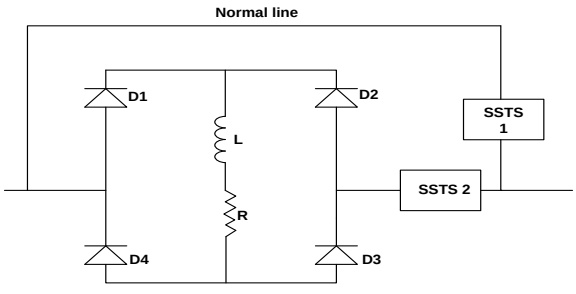


Figure 5: Switch Based Fault Current Limiter (SFCL).

PROPOSED COMPOUND METHOD

Consider Figure 4 as part of a distribution network which contains a critical load. There is not any FCL in the system. The critical load requires the uninterrupted electrical power with very high quality. If a fault occurs at line 1, the circuit breaker operates and the faulty line separates from other part of the system. But the circuit breaker has a time delay before its action. During this time delay, Vpcc decreases, so the critical load is fed by the electrical power which has very bad quality, hence the operator should compensate the critical load.

At first, it is assumed that a shunt custom power device such as DSTATCOM is used for compensating the critical load to improve power quality. The amount of injected current of the shunt device can be computed by equation (1). As mentioned earlier, the rate of voltage of the shunt inverter is equal to the rate of voltage of the critical load, so the maximum required Volte-Ampere (VA) for compensator can be calculated by multiplying the rate of voltage and the maximum injected current.

Now consider a series compensator such as DVR which is used to improve power quality of the critical load. After a fault and before circuit breaker action, the custom power should inject a series voltage to the system to improve power quality. The amount of injected voltage can be calculated by Equation (2). To compute the stored energy for compensating the voltage drop, the magnitude of voltage drop should be multiplied to the current of load and the period of voltage drop.

Paying attention to Equations (1) and (2), it is obvious that by decreasing the amount of voltage drop and THD, the required voltage in the series compensation or current in the shunt compensation which should be injected to system will be reduced. It means that the rate of required power and so the cost of compensator will be reduced.

Now consider the proposed SFCL has been installed at line 1. Before the fault occurs, the SSTS1 is on and SSTS2 is off, so the SFCL is at the OFF-state and both of the loads are fed by the infinite bus with high power quality. When a fault takes place at line 1, the SFCL will come ON very fast and very high impedance will appear in line 1 and limit the current of fault. Therefore, after the fault condition and before circuit breaker

action, the SFCL reduces the voltage drop at the point of common coupling (Vpcc). The SFCL is also able to decrease the THD of the voltage and current of the critical load. As mentioned before, the required power rating and therefore the cost of custom power device which is used for compensating can be reduced by using the combination of the SFCL and DFACTSs. It is noticeable that the price of the proposed SFCL is very lower than the devices such as DVR and DSTATCOM.

CASE STUDY

In this section the proposed technique has been tested on a distribution system which is shown in Figure 6. The system consists of two loads and two feeders. An uninterruptible infinite bus supplies power demand of the system through a 138/33 KV transformer. The parameters of the system are given in the Appendix.

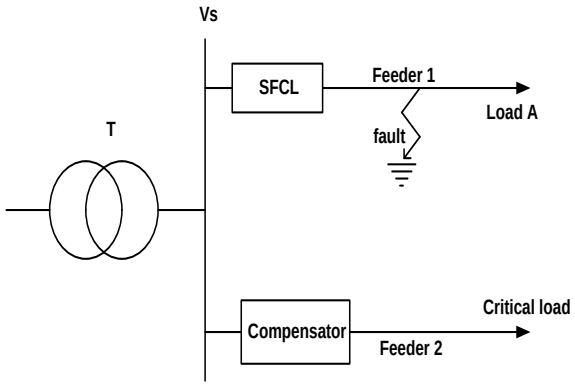
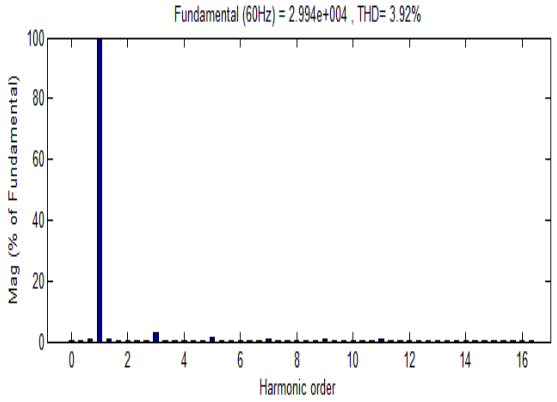


Figure 6: Diagram of the Study System.

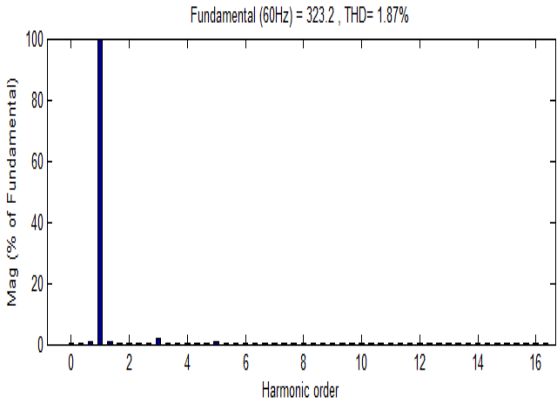
In this paper, it is assumed that before the fault condition, the voltage sag and total harmonic distortion (THD) of voltage of load A should be kept less than 10% and 4%, respectively. Also, for the critical load, before and after fault occurrence, the voltage sag and total harmonic distortion (THD) of voltage and current should not exceed from 3% and 1%, respectively.

At first, consider the system operator uses an FCL which cannot change its state (Figure 5 without SSTS1 and SSTS2). Since the voltage sag and THD of load A should be less than 10% and 4%, the impedance of FCL should not be set very large. In this simulation, R_{FCL}=2.4Ω and L_{FCL}=0.04H.

Figure 7 shows the harmonic analysis of voltage and current of load A before the fault condition which have acceptable quality.



(a)

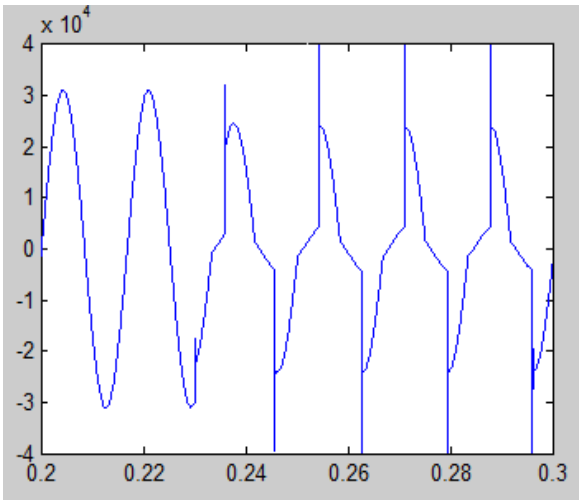


(b)

Figure 7: The Harmonic Analysis of (a) Voltage and (b) Current of Load A before the Fault Using FCL.

Consider a fault which occurred at t = 0.23 sec and the circuit breaker separated the faulty section (feeder 1) from bus s after 0.07 sec. The time duration of the fault is assumed to be 300 msec.

Figures 8 and 9 depict the simulation results for critical load when the system operator uses the FCL. Figure 8 shows the waveforms of the voltage and current of critical load which their qualities are not acceptable. Figure 9 shows the harmonic analysis of voltage and current of critical load after fault occurrence and before circuit breaker action.



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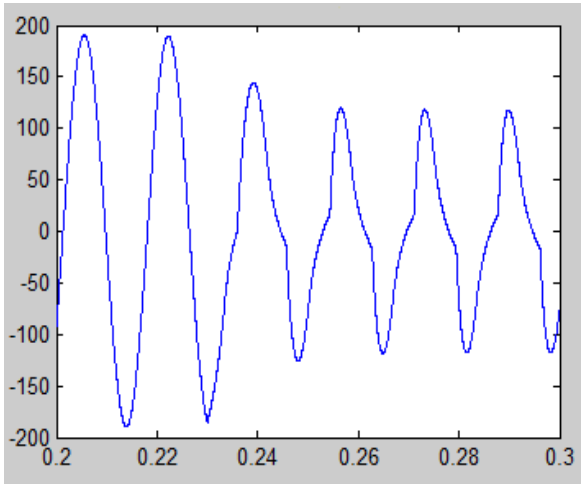
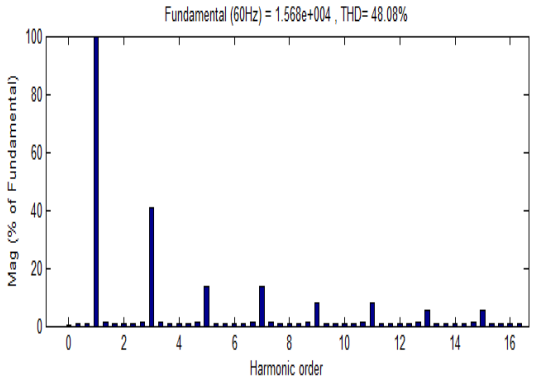


(b)

Figure 8: The Waveform of (a) Voltage and (b) Current of Critical Load after Fault Using FCL.

The THD and amplitude of the fundamental frequency for the voltage and current are 48.08%, 26.86%, 15.68KV, and 96.29A, respectively.

Therefore, the critical load should be compensated after the fault occurrence. Depending on the system conditions and the necessity of critical load, the series or shunt DFACTSs can be chosen by the system operator to be installed near the critical load. Table1 shows the features of series and shunt compensators which can be installed to improve the power quality of the critical load.



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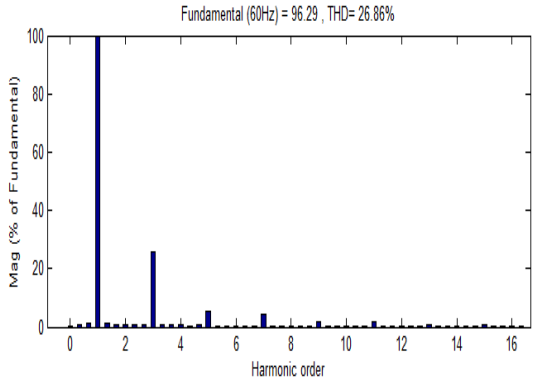


(b)

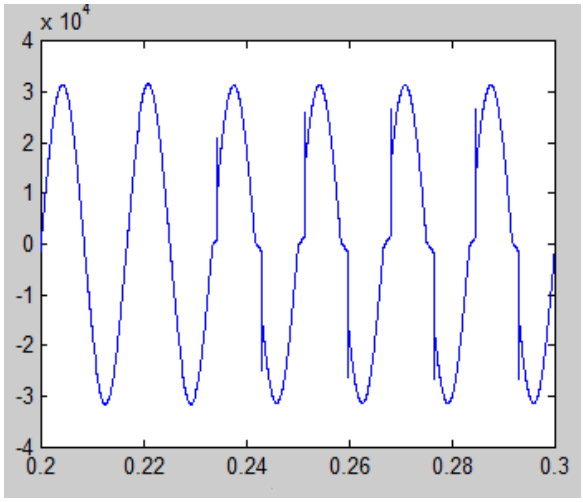
Figure 9: The Harmonic Analysis of (a) Voltage and (b) Current of Critical Load after Fault Using FCL.

Table 1: The Required Features of Series and Shunt Compensator Using FCL.

	V_{inject} (KV)	I_{inject} (A)	Required power (MVA)
Series compensator	23.49	–	2.351
Shunt compensator	–	51.20	1.690

Now consider the system operator uses the proposed SFCL. Before the fault occurrence, SSTS1 is on and to feed load A, the electrical power does not cross through the FCL. Hence, the impedance of FCL can be set very large. After fault condition, SSTS1 and SSTS2 will become off and on, respectively.

In this situation the large impedance comes in to the system and limits the current of fault and reduces the percentage of voltage dip and also THD. In this simulation, R_{FCL}=50Ω and L_{FCL}=0.4H. Figures 10 and 11 depict the simulation results for the critical load after fault and before circuit breaker action. Figure 10 represents the waveform of the voltage and current of critical load and Figure 11 shows their harmonic analysis. The THD and amplitude of the fundamental frequency of the voltage and current are 11.94%, 5.20%, 30.91KV, and 188.2A, respectively.



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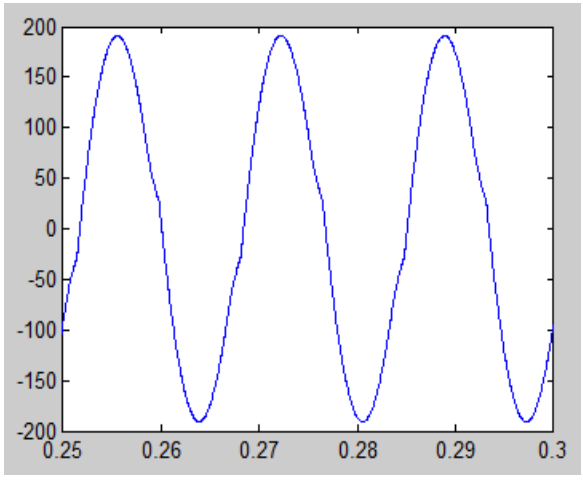

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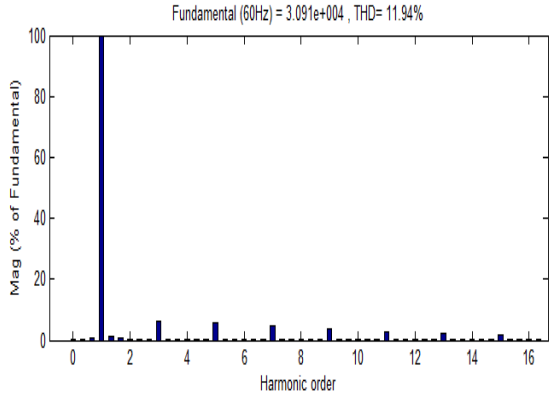
Figure 10: The Waveform of (a) Voltage and (b) Current of Critical Load after Fault Using SFCL.



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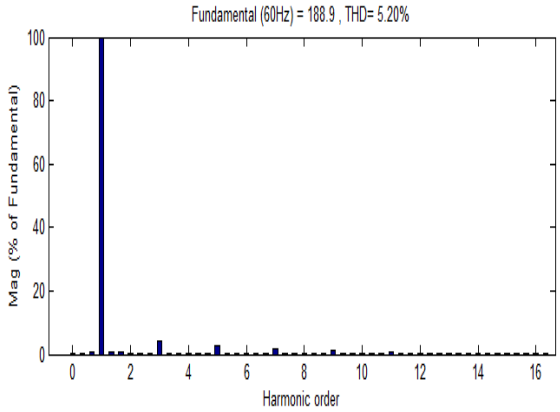

(b)

Figure 11: The Harmonic Analysis of (a) Voltage and (b) Current of Critical Load after Fault Using SFCL.

With comparison between Figures 8, 9, 10, and 11 it is clear that by using the proposed SFCL instead of FCL, the voltage and current of critical load after fault occurrence have better quality. It is noticeable that after the fault condition, the amplitude of fundamental frequency and the THD of voltage and current of critical load should be less than 3% and 1%. Therefore, the system requires compensation. As mention before, the kind of compensator which the system operator should install depends on the system conditions and necessities of the critical load.

Table 2 represents the features of series and shunt compensators which can be installed to enhance the power quality of the critical load.

Table 2: The Required Features of Series and Shunt Compensator Using SFCL.

	V_{inject} (KV)	I_{inject} (A)	Required power (MVA)
Series compensator	4.46	–	0.446
Shunt compensator	–	43.89	1.448

Comparison between Tables 1 and 2 shows that when the operator uses the SFCL, the injected voltage (series) and current (shunt) and also the required power rating of compensator will be decreased in contrast to using FCL. Therefore, the cost of custom power device which should be installed near the critical load will be reduced.

CONCLUSION

Due to the increase in using nonlinear loads in power systems, power quality improvement has become a very important topic over the past several decades. Custom power devices are a kind of FACTS devices which are used in distribution networks to enhance power quality. The cost of custom power devices depends on their power rating and size. This paper has shown a method based on using the combination of a switch based fault current limiter (SFCL) and custom power device to decrease the required power rating of series and shunt compensators, therefore reducing the investment cost of compensation. The proposed SFCL does not have any bad effect on power quality of the loads which are placed after it and is able to mitigate voltage sag and reduce the total harmonic distortion of voltage and current of the critical load.

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APPENDIX

Transformer data:
138/33 KV, 15 MVA, 0.08 pu

Data of feeder 1:
Length of feeder = 5 km
Reactance= 0.12 Ω/km
Resistance= 0.1 Ω/km

Data of feeder 2:
Length of feeder = 9 km
Reactance= 0.2 Ω/km
Resistance= 0.25 Ω/km

Data of load A:
Power factor= 0.85
Active power demand= 5 MW

Critical load data:
Power factor= 0.9
Active power demand= 3 MW

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